DEVELOPMENT OF A DIGITAL LLRF CONTROL SYSTEM AT LNL

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Abstract

The new Low-Level Radio Frequency (LLRF) control system for linear accelerator at Legnaro National Laboratories (LNL) of INFN is presently being commissioned. A digital Radio Frequency (RF) controller was implemented. Its goal is to stabilize the amplitude, the phase and the frequency of the superconducting cavities of the Linac. The resonance frequency of the low beta cavities is 80 MHz, while medium and high beta cavities resonate at 160 MHz. Each RF controller controls at the same time eight different cavities. The hardware complexity of the RF controller (RF IOC) is reduced by adopting direct RF sampling and the RF to baseband conversion method. The main hardware components are RF ADCs for the direct undersampling of the signals picked up from cavities, a Xilinx Kintek 7 FPGA for the signal processing and DACs for driving the power amplifiers and hence the cavities. In the RF IOC the serial communication between FPGA and ADCs and between FPGA and DACs is based on JESD204b standard. An RF front-end board (RFFE) is placed between cavities and the RF IOC. This is used to adapt the power level of the RF signal from the cavities to the ADCs and from the DACs to the power amplifiers. This paper addresses the LLRF control system focusing on the hardware design of the RF IOC and RFFE boards and on the first test results carried out with the new controller.

INTRODUCTION

The superconducting linear accelerator ALPI [1] requires a significant RF field stability in phase, amplitude and frequency to ensure the best energy gain of the accelerated beam. The resonance frequency of a first group of ALPI cavities is 80 MHz, while that of a second group is 160 MHz. The cavities act as filters, with an high quality factor. In order to keep the RF field stable in the cavities, amplitude and phase have to be controlled to compensate the impact of microphonic perturbations.

RF CONTROLLER

In order to improve the stability of the RF field in the cavities a new RF control system has been developed [2]. The new digital RF controller system has been designed exploiting the performances of commercial components like RF ADCs, FPGA and DACs. It is based on direct sampling of RF signal and digital signal processing with FPGA. This allows a greater flexibility in programming and diagnostic capabilities, since it is possible to monitor many signals during the processing of the data inside the FPGA, like amplitude and phase of the RF fields in cavities.

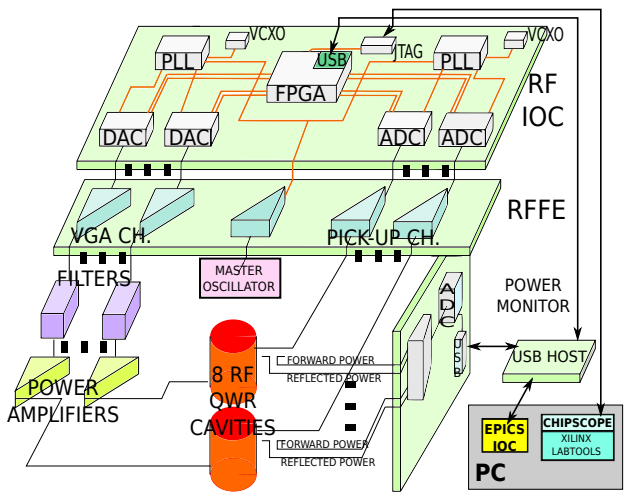

Figure 1: Block diagram of the LLRF system.

A block diagram of the LLRF control for the cavities is represented in Fig. 1. It is based essentially on three boards: the RF input-output controller (RF IOC), the RF front end (RFFE) and the power monitor that measures the reflected and forward powers of the eight controlled cavities. These boards are housed in a single box as shown in Fig. 2. In the RF IOC the signals coming from the cavities are amplified through the RFFE board and then undersampled and digitized. These signals are digitized using the IQ method. As reported in [2] the sampling rate of the ADCs has been chosen so that $f_s = D \times 4 f_{RF}/(4 \times k + 1) = 121.9$ MHz, with D the decimation factor, f_{RF} the resonance frequency and $k = 5$. After processing in the FPGA, the signals are reconverted in analog form, filtered by Helical Resonator filters, amplified via the RFFE and sent to the power amplifiers. To simplify PCB design the communication between FPGA and converters is based on JESD204b serial interface. The control algorithms described in [2] are implemented in the FPGA and written in VHDL code. Fixed-point arithmetic has been preferred over floating-point arithmetic because of its convenience in FPGA implementation.

RF IOC

The RF IOC, Fig. 3, is essentially composed of four high linearity dual channel 16-bit, 250 MSPS analog-to-digital converters ADS42JB69, a Xilinx Kintek 7 FPGA in which the LLRF logic is implemented using VHDL code and four

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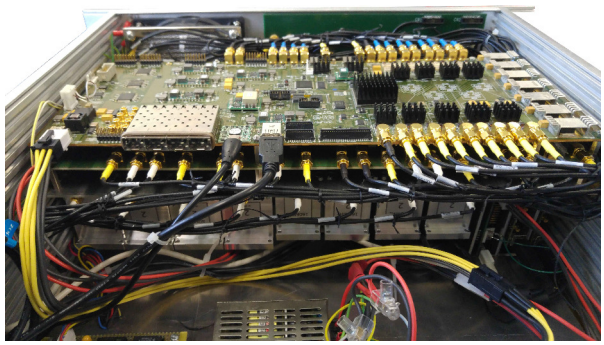
(a)



(b)

Figure 2: Box (Octal Resonator Controller) containing the RF IOC, the RFFE, eight helical resonator filters and the power monitor board(PM). (a) Front view: in foreground the front panel and the RF IOC. (b) Back view: the stack composed by the RF IOC, the RFFE, the eight filters and, on the bottom right corner, the power monitor.

high-speed, high-performance 16-bit dual channel Digital-to-Analog Converters DAC1658D. Both ADCs and DACs support a JESD204b compatible high-speed serial input data interface. The clock signals are generated by two clock jitter cleaner LMK04828. The first stage of the PLL is driven by a 160 MHz reference signal provided by the master oscillator at ALPI. An external VCXO at 100 MHz provides the reference clock for the second stage of the PLL. ADCs, DACs and PLL feature an SPI slave interface to access their internal registers. The output of the PLLs can be configured to drive up to seven JESD204b converters.
The physical layer of the JESD204b standard serial communication is devoted to transmission and reception of characters bit. In the FPGA this layer and the 8B/10B encoding and decoding has been implemented using GTX transceivers. Since we are not interested in the deterministic latency of the link between the FPGA and the data converters, we have used JESD204b subclass 0. This choice minimizes the interface hardware complexity. Both ADCs and DACs are configured to operate with two lanes per single converter.

RF Front End

The RFFE, Fig. 4, is basically composed by eight sections, one for each controlled cavity.

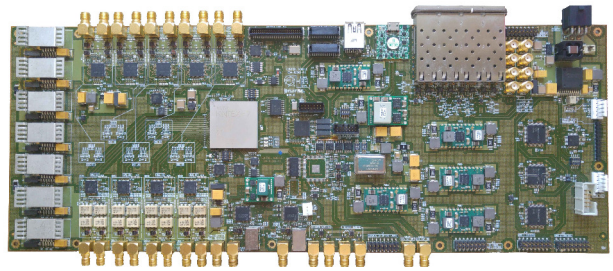


Figure 3: Radio Frequency Input/Output Controller board (RF IOC).

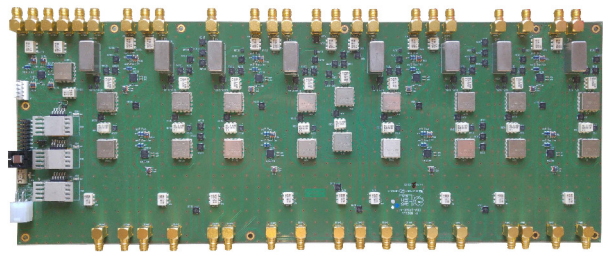


Figure 4: Radio Frequency Front End board (RFFE).

Each of these sections is split into two channels:

- the pick-up channel. It is used to match the power level of the signal picked up from the cavity to a suitable value to be sampled by RF ADCs. This gives us 45 dB of dynamic range.
- the VGA channel. It is used to amplify the signal coming from the DACs. It consists of the low noise voltage gain dual IF amplifier. The two amplifiers are cascaded to have a 62 dB gain control range.

The RFFE board programmable components are configurable through the RF IOC using the serial I2C protocol.

TESTS AND MEASUREMENTS

Both off-line and on-field test measurements have been taken with a RF IOC prototype and a RFFE prototype. The off-line measurements here reported concerns the sampling clock signals of the ADCs and the isolation between channels in the RFFE.

The ENOB of the ADCs affects the measurement sensibility of the RF field in the cavity. This parameter is strictly related to the jitter of the clock signal used to sample the ADCs input. Clock waveform and Time Interval Error (TIE) histogram are shown in Fig. 5. From the histogram one can deduce that the jitter has a deterministic component. Looking at the waveform of the clock in the time domain a ringing due to reflections is visible. After careful investigation we found the presence of improper impedance termination and physical media discontinuities in clock transmission lines. This contributes to decrease the ENOB of the ADCs.

The scattering parameter S_{21} is a good estimator of the cross talk between adjacent channels in the RFFE board. In Fig. 6 the blue trace represents the magnitude of the S_{21}

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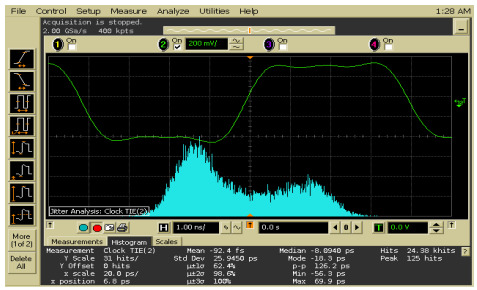


Figure 5: Clock signal of the ADCs.

when the aggressor is the pick-up channel and the victim is the next VGA channel of the same section. The red trace of Fig. 6 represents the magnitude of the S_{21} parameter when the victim is the VGA channel of the next section. The magnitude of the scattering parameter at the working frequencies 80 MHz and 160 MHz is less than −50 dB.

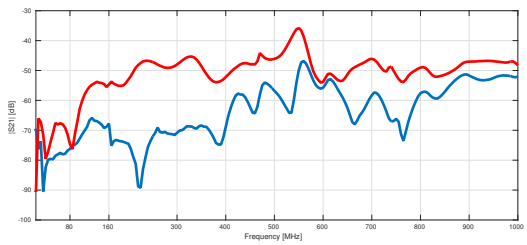
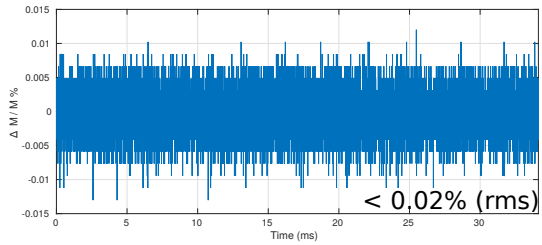


Figure 6: Magnitude of the scattering parameter S_{21} vs. frequency.

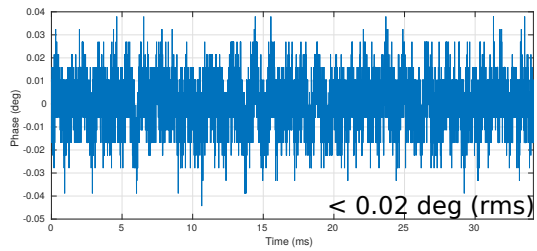
The performance of the prototype RF control system has been tested by measuring the amplitude and phase errors using four cavities at 80 MHz and four cavities at 160 MHz in superconducting conditions. The phase and magnitude stability were evaluated with an accelerated beam current of nA of ^{32}S and eight cavities phase and amplitude locked. Throughout the testing sessions, the magnitude and phase loops were closed in Self Excited Loop (SEL) mode. Fig. 7a shows the relative magnitude error during SEL operations for a medium beta cavity. The relative magnitude error is $1.54 \cdot 10^{-4}$ rms. Fig. 7b shows phase error for a medium beta cavity. The phase error is 0.019 degrees rms. The robustness of the feedback control loop, in phase and in amplitude margins was checked in on-field test. This was done studying the step response of the RF field in the cavity changing the setpoints in amplitude and phase. The transient analysis are shown in Fig. 8 for a medium beta cavity.

CONCLUSIONS

A prototype RF controller of the new LLRF system of the ALPI has been presented. It has been used to keep eight cavities phase and amplitude locked for a few days. The results of measurements and signal processing show excellent agreement of phase and amplitude field stability requirements for modern linear accelerators. An excessive clock jitter has been measured in the controller board. It is advisable to reduce the jitter with a careful clock distribution network on the printed circuit board in the next revision of the controller board.



(a)



(b)

Figure 7: Field magnitude error (a) and phase magnitude error (b) for a medium beta cavity running in SEL mode.

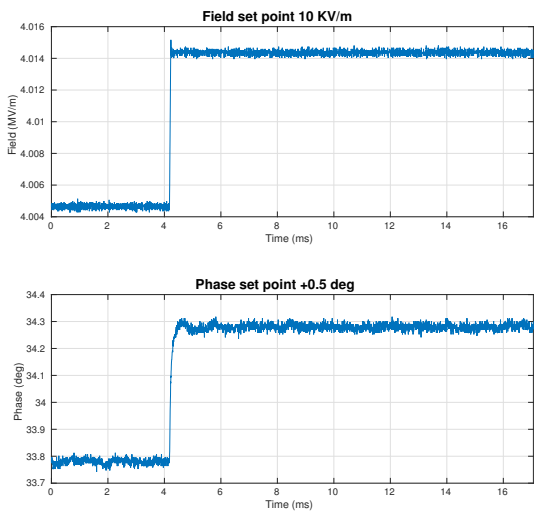


Figure 8: Step response of the field magnitude (a) and of the phase (b) for a medium beta cavity.

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