PULSED HIGH POWER KLYSTRON MODULATORS FOR ESS LINAC BASED ON THE STACKED MULTI-LEVEL TOPOLOGY

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Abstract

ESS has launched an internal R&D project in view of designing, prototyping and validating a klystron modulator compatible with the requirements based on a novel topology named SML (Stacked Multi-Level). This topology is modular and based on the utilization of High Frequency (HF) transformers. The topology allows for the usage of industrial standard power electronic components at the primary stage at full extent which can easily be placed and wired in a conventional electrical cabinet. It requires only few special components like HF transformers, rectifiers and filters (i.e. passive components) to be placed in an oil tank. This arrangement allows scaling up in average and pulse power to the required levels while keeping the size, cost, efficiency and reliability of the different modules under good control. Besides the very good output pulse power quality, the AC grid power quality is also remarkably high with a line current harmonic distortion below 3%, a unitary power factor and an extremely reduced line voltage flicker below 0.3%. A reduced scale modulator prototype has been built and validated experimentally.

INTRODUCTION

The European Spallation Source is a multi-disciplinary research facility in the field of materials science currently under construction in Lund, Sweden. The spallation process will be achieved thanks to utilization of the world most powerful Linac which will provide 2.86 ms long proton pulses at 2 GeV at a pulse repetition rate 14 Hz, representing an average beam power of 5 MW in the target (Fig. 1) [1].

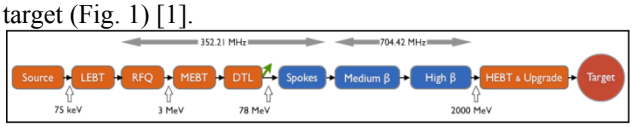

Figure 1: ESS linear accelerator layout.

The Linac will require, amongst others, the following High Power RF amplifiers:

- 1 Klystron for the RFQ;
- 5 Klystrons for the DTL tanks;
- 36 Klystrons for the Medium Beta;
- 84 Klystrons or IOT's for the High Beta

Due to the pulsed nature of the Linac, all klystron modulators will also be pulsed with a pulse width of 3.5ms, allowing for RF stabilisation and filling time of the cavities.

In order to save costs and reduce the footprint on the RF Gallery, largely influenced by the modulators, ESS has decided to launch an internal R&D project in collaboration with Lund Technical University for the development of modular high power modulators able to power up-to 4 klystrons in parallel, each rated for1.2MW RF.

These requirements translate into an electrical pulsed power of 11.5MW to be delivered by each modulator and an average power, absorbed from the AC grid, of 660kVA.

The following powering scheme has been adopted:

- Mod. #1: RFQ & DTL tank #1 klystrons in //;
- Mod. #2, #3: DTL tank #2,#3 & #4,#5 klystrons;
- Mod. #4..#12: Medium Beta klystrons;
- Mod. #13..#33: High Beta klystrons or IOT's;

All modulators are expected to be identical in their ratings, topology and interfaces.

On the contrary of many Linac components like klystrons, RF cavities, RF distribution systems including waveguides, magnets, vacuum systems, cryogenics, etc. that once designed for the peak power depend very slightly on the machine average power, the modulators which have to produce the peak power at their outputs and absorb a constant average power at their inputs represent one of the most challenging pieces of equipment. The challenges consist mainly in combining high pulse power, fast rise-times, high flat-top accuracy and AC grid power quality (low current harmonic distortion, very low flicker). These requirements, once combined with a compact design, low cost per kW peak and kW Average and high reliability, contribute to a worldwide unique set of specifications that led to the development of a novel topology called Stacked Multi-Level (SML), which is described below.

ESS MODULATOR REQUIREMENTS

Table 1 summarises the main requirements of the ESS klystron modulators. Additionally, the following design goals have been identified as crucial to achieve the above mentioned objectives and were on the basis for the SML topology choice:

- Safety, health and environmental sustainability (safe and reliable energy storage; biodegradable dielectric materials);
- Highly demonstrated and qualified power semiconductors (like IGBT's), power stacks and passive power components (inductors, capacitors) for higher reliability;
- Easy accessibility to components for maintenance and easy replacement of modules (MTTR < 3 hours);

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- Small footprint (width: <4m; depth: <1.4m; height: <2.4m) and weight (total: <8 ton; per component: <2 ton);
- Cost effectiveness due to modular production and the utilization of standard components into a maximum extent, of at least double sources;

Table 1. Main Requirements of ESS Klystron Modulators

Pulse voltage amplitude, U_N	-115kV
Pulse current amplitude (total for 4 klystrons in //)	100A
Pulse length (50% amplitude)	3.5ms
Pulse repetition rate:	14Hz
Max. pulse rise time (0..99%)	120µs
Max. pulse overshoot	2% of U_N
Max. pulse reverse (backswing) voltage	10% of U_N
Max. voltage droop on pulse flat-top	1% of U_N
Max. voltage ripple on pulse flat-top	0.15% of U_N
AC grid line voltage	600V
Max. flicker on AC grid	0.3% of U_N
Max. current THD on AC grid	3%
Min. efficiency, AC grid to HV output	90%

PULSE TRANSFORMERS VS HIGH FREQUENCY TRANSFORMERS

Conventional solid state modulators typically use HV pulse transformers to perform voltage amplification (Fig. 2a). In these topologies, a medium voltage capacitor charger charges a capacitor bank and a solid state switch discharges it into the primary of the transformer which steps up the voltage to the level required by the klystron [2]. The size and weight of such transformers are highly impacted by the pulse width, the pulse power and the rise time. In the case of ESS, the combination of all these parameter requirements would lead to a bulky device [3].

An alternative is the utilization of a HF pulse modulation/demodulation scheme using HF transformers (Fig. 2b). In these topologies, a fast DC/AC inverter generates a low voltage AC square-wave voltage from the pre-charged DC capacitor bank. This HF wave can then be transmitted through a dedicated transformer that operates in AC instead of pulsed mode; its size being reduced with the switching frequency increase. At the secondary, a diode bridge rectifier and low pass filter will reconstitute the original pulse shape although amplified by the transformation ratio. The size and weight of the HF transformer is very weakly dependent on the pulse width.

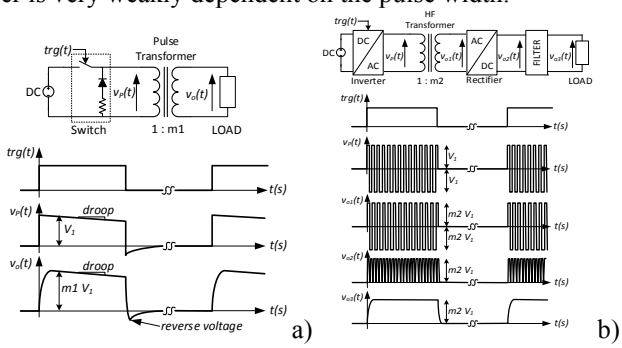

Figure 2: Pulse voltage amplification based on: a)- Pulse transformer; b)- HF transformer.

STACKED MULTI-LEVEL TOPOLOGY

The Stacked Multi-Level (SML) topology exploits the High Frequency modulation/demodulation principle described above but introducing modularity by stacking several modules in series at the output stage (to further multiply the voltage by the number of modules N) and by connecting several capacitor chargers in parallel at the low voltage AC grid stage.

Furthermore, this topology utilises the concept of Active Front Ends (AFE) [4] well known from industrial applications like motor drives and photovoltaic inverters in order to improve the AC power quality. The DC/DC buck converters placed after the AFE's charges the capacitor banks at constant power, therefore avoiding flicker on the AC grid.

Fig. 3 shows the complete topology adopted [5]. Depending on the application power and voltage levels, the number of each module type can be adjusted without risking "cross talking" between them.

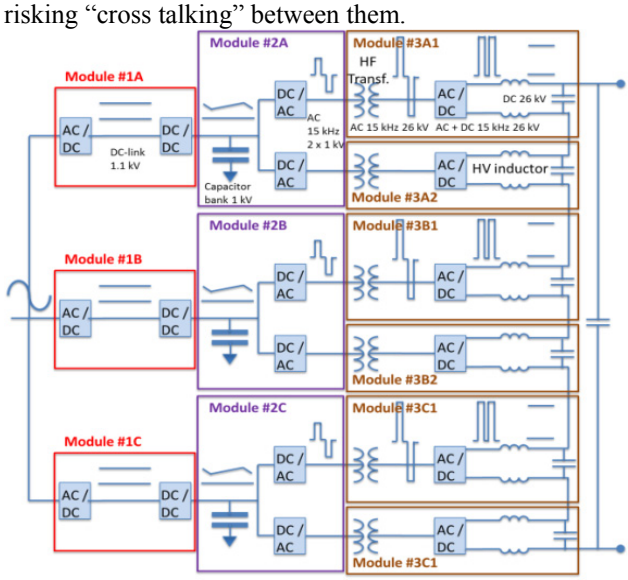

Figure 3: SML topology optimised for ESS modulators.

EXPERIMENTAL RESULTS OBTAINED ON A REDUCED SCALE PROTOTYPE

A Reduced scale prototype was designed and built to prove the concept and their implementation techniques [5]. It was rated for all same parameters of the full scale system (Table I) but rated for 1/5th of the output current. Since the average power is only 130kVA, a standard 400V AC line was used for the input.

The DC/DC converters on the modules #1 A,B,C are controlled via conventional PWM from a current regulation loop. The reference of this current loop is calculated as the reference charging power divided by the measured capacitor voltage. This way, the actual charging power is permanently regulated during the entire pulsing cycle (including during the HV pulse generation period and the standstill period between HV pulses). The power reference is then computed over one entire pulse cycle in order to allow achieving the required capacitor voltage precisely at the instant when the next pulse is starting. This

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scheme is the key for effective power regulation at the input of the DC/DC (load for the AC/DC) and for flicker free operation.

Additionally, the AC/DC AFE's are regulated on a conventional way, i.e. regulating the intermediate DC-link bus voltages while simultaneously regulating the AC line current on the grid.

The corresponding waveforms are shown in Fig. 4. It can be observed that the AC line current is sinusoidal, in phase with the line voltage (i.e. unitary power factor) and has a constant amplitude and shape (no flicker). The charging current waveform provided by the DC/DC stage has a pattern such that once multiplied by the capacitor bank voltage, the resulting product is constant over time, therefore confirming a constant power regulation.

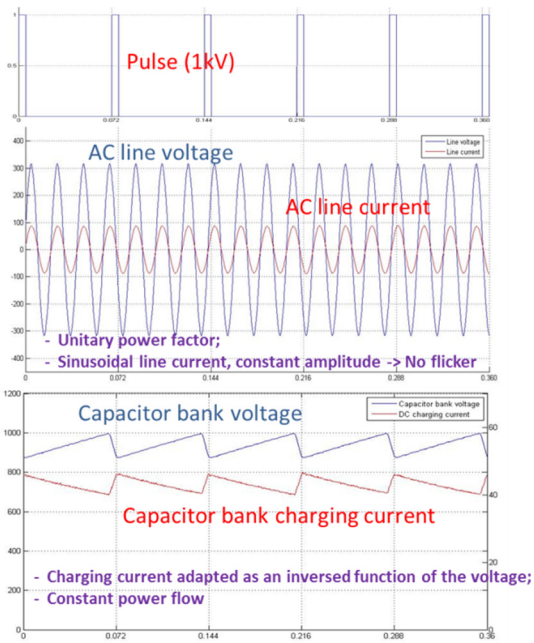

Figure 4: AC line current, capacitor bank voltage and charging current in pulsing mode (experimental).

660KVA SML MODULATOR LAYOUT

Figure 5 shows the output HV pulse and primary voltage and current on one HF transformer. The rise time (0..99%) is in the order of 120µs and the droop is below 1%. The HF modulation of the transformer primary voltage during the pulse duration is also illustrated.

Figure 6 shows the 3D model of the complete 660kVA modulator based on the SML topology of Fig. 3. The HV oil tank assembly is located on a metallic frame with wheels for easier transportation. On top, the LV power electronics containing all components up-to the primary of the HF transformers is placed in a second similar frame. When assembled, the whole system behaves as a single block and can be transported as a single unit.

Figure 7 shows the interior of the HV oil tank assembly where the 6 HV modules are sitting. Each of these modules is powered up from a H- bridge inverter placed in the top frame just above the transformer connection terminals.

Figure 8 shows details of one HV module, formed by one HF transformer and one HV rectifier box.

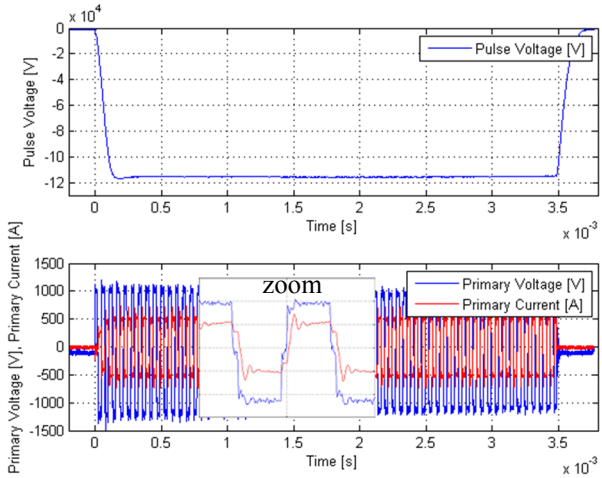

Figure 5: HV pulse waveform and primary voltage/current on one HF transformer (experimental).

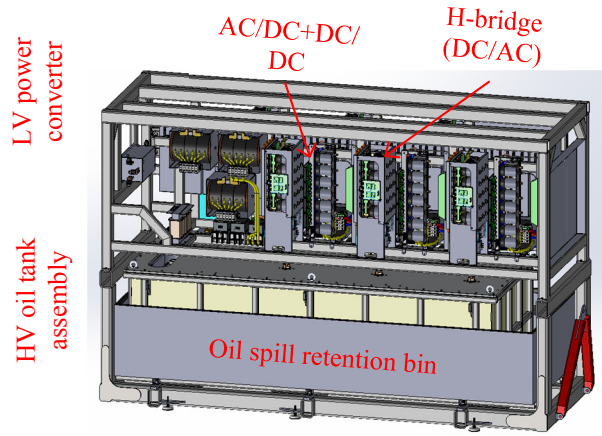

Figure 6: 3D layout of the complete 660kVA SML modulator (Size: 3.8m x 1.4m x 2.5m).

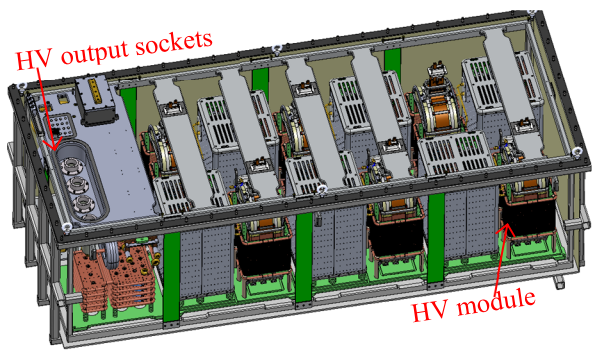

Figure 7: 3D layout of the HV oil tank assembly.

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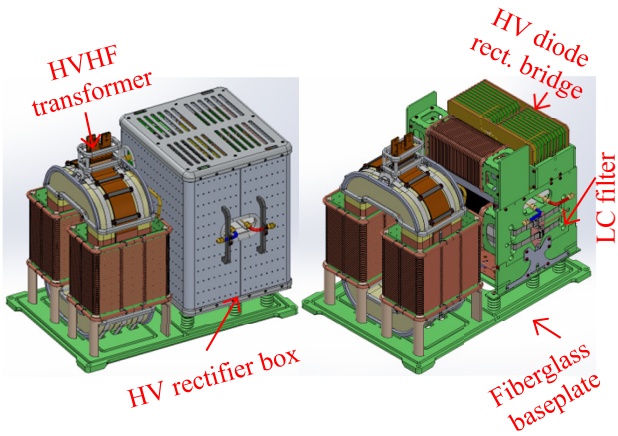

Figure 8: 3D layout of one HV module.

Over approximately 1 year of operation of the LV power converter stage no false trips due to noise or failure of main components has occurred. Furthermore the complete prototype was subject to a consecutive 12 hours heat run test at nominal parameters with success.

CONCLUSION

The SML topology has been developed and validated experimentally as an alternative to conventional pulse transformer based topologies. The test results obtained with a prototype show a HV pulse waveform with amplitude of 115kV/20A, a rise time below 120µs and a droop below 1%. Simultaneously, it revealed excellent power quality on the AC grid side with nearly sinusoidal current absorption and flicker free operation, thanks to the association of an AFE and a DC/DC constant power regulated buck converter.

The design of the full scale series units, rated for 660kVA, allowing powering up to 4 klystrons in parallel rated for 1.4MW RF has confirmed the construction feasibility using only standard components in the LV power converter stage and conventional materials (i.e. fiberglass, diodes, capacitors, nanocrystaline cores) in the HV oil tank assembly, although with customised machining for a compact still with relatively simple assembling procedures.

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