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PERFORMANCE TEST RESULTS OF MAGNET POWER SUPPLY*

K. H. Park†, S. H. Jeong, Y. G. Jung, D. E. Kim, H. S. Suh, H. G. Lee, S. B. Lee, B.G. Oh, M. J. Kim and J. H. Han, PAL, POSTECH, Pohang, Korea

Abstract

A high stable magnet power supply (MPS) was developed, which was a bipolar type with 200 A of the output current at the 36 V of output voltage. The MPS has been implemented by the digital signal processing technology using the DSP, FPGA, ADCs and so on. The output current stability of the MPS showed about 6 ppm peak-to-peak in a short term experiment at its full 200 A output current. The long term stability was shown in 15 ppm peak-to-peak for 10 hours at 200 A. And the others experimental results about the MPS were shown in this paper.

INTRODUCTION

The particle accelerator needs a highly stable magnet power supply (MPS) to assure the stable beam dynamics. A MPS must provide high-stability output current, fast response, high reliability, etc. It should also be easy to maintain. The stability and accuracy of the MPS are very important specifications because they directly affect the beam dynamics of the accelerator operation. Nowadays the MPS is developed by switching mode type using FET or IGBT devices that are controlled by a digital signal processor (DSP). This design is efficient, small, light-weight, and has good dynamic response but switching-mode MPS generates electrical noises whenever switching devices are turning on or turning off because of their generally high switching voltage and current. The short-term stability of the MPS is affected by the several causes which come from the control loop responses, surrounding switching noise, analog signal processing including ADC circuits, and so on [1]. Ripple components of the input rectifier are also one of the sources which make MPS stability worse [2]. The one of the cause of the long-term stability of the MPS comes from the temperature drift of components in MPS. Improper ground configurations can provide the path on which noise can propagate from its source point to all over the system. These components are very small but can degrade the performances of an analog-to-digital converter (ADC) circuits with the fine voltage fluctuation.

This paper describes the design schemes of the MPS. The results of the various experiments such as short term stability, long term stability, repeatability and step responses were showed.

SYSTEM CONFIGURATION

The developed MPS was divided into three parts as shown in the Fig. 1. The first is a rectifier to make DC link voltage. The second is the two power stacks which has the current driving capacity of 100 A, respectively. Thus two power stacks are operated in parallel to increase the current driving capability. The last is digital controller configured with DSP TMS320F28335 from TI [3].

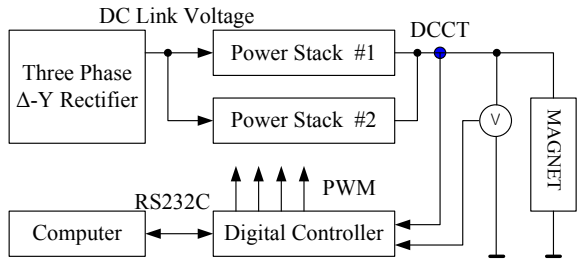

Figure 1: The block diagram of the developed MPS.

The rectifier to make DC link voltage with low ripple components was assembled. The primary winding of the transformer was configured with three phase in Wye configuration for AC 380 V. The secondary winding is consisted of two configurations of the Wye and Delta. The output voltage of the each winding on the secondary side is 33 V, respectively. They are fully rectified by the twelve diodes and connected in series to make DC link voltage of 66 V. Two diode modules of SEMIX341D16s from SEMICRON Co. were assembled on the water cooled aluminium plate. The input rectifier has an inductor of 1 mH to compose the input filter with the capacitor bank, 12000 μF x 4, in two power converter modules, respectively.

The performances of the ADC were very important part for the high stable MPS. The circuits of around ADCs for the MPS should have a good signal to noise ratio. The major specifications when the ADC was chosen were the throughput, resolution, input range, interface, DC accuracy, and so on [4]. Two different types of ADCs were tested to confirm their performances under the same conditions. The first one is the AD7690 from Analog Devices that is 18-bit resolution. The tested effective resolution of this ADC showed only 10-bit. The 8-bit in 18-bit was meaningless. The last one is the AD977 from also Analog Devices showed the effective resolution of 12-bit in spite of the 16-bit resolution in the given specification. These test results showed sometimes worse resolution than that of the datasheets. It might be depended on design scheme of the ADC and the conditions around circuits such as reference voltage source type, supply voltage and ground conditions, etc. The higher resolution than 16-bit in ADC may be meaningless because the ground thickness was about 1mV in general analog and digital mixed circuits. It was corresponding to nearly 1-bit at 10 V reference voltage.

Two types of ADC daughter boards for the MPS were developed as in the Fig. 2. The type 1 ADC board was to

*Work supported by Ministry of Science and ICT
†pkh@postech.ac.kr

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digitize the load current or voltage for the feedback control loop. This type was designed by combining two ADCs that sampled the input signal simultaneously, which increased the SNR by the over-sampling technology. The type 2 ADC board for other purposes such as heat sink temperature, link voltage, etc. was assembled with one ADC and analog multiplexer as the bottom side at the Fig. 2. The interface signals between FPGA and ADC were isolated using the digital isolators ISO7241 from TI. And the DC power supply for the each ADC daughter board was also isolated to minimize the noise coupling through the ground or power plane in the PCB.

Figure 2: ADC daughter boards for current and voltage for feedback control (upper) and general purpose (lower).

The interfaces among the devices of the MPS were shown in the Fig. 3. The ADCs up to seven and a DAC were interfaced by the SPI to the FPGA. The DSP and FPGA were assembled in a board. The interface between them uses a Multichannel Buffered Serial Port of the DSP peripheral. The ADC data were transferred to the DSP whenever the DSP sends the designated signal to the corresponding ADC channel. The MMI was composed by the Labview and communicated by the RS232C. The Easy-DSP which is the tool for downloading program and monitoring the variables in real time was also connected by another RS232C.

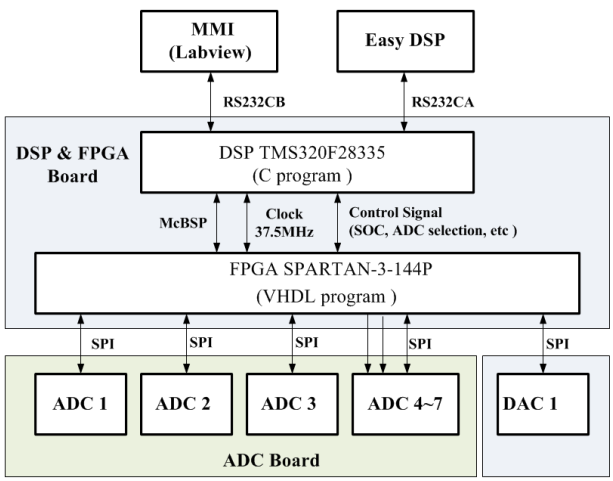

Figure 3: Interface signals between devices in the MPS.

The feedback control signals, load current and voltage, were sampled every 200 kHz by the FPGA. These data were moving-averaged out with the stored data in the FIFO buffer at the FPGA SPARTAN-3 from Xilinx [5]. The functions in VHDL program were written by modular type, so it was easy to modify. And the functions in FPGA were processed in parallel, so program execution time was not issue here. The data were always ready to send to the DSP whenever requested. The DSP program was divided into two parts. The one is interrupt routine which is generated at every PWM frequency, 15 kHz, to calculate the duty ratio for the IGBT control. The other is the base routine that scans the interlock signals and RX buffer of the RS232C for the MMI as shown in the Fig. 4. The interlock signals like the IGBT failure directly make the PWM signals disable by the hardware which is programed in the CPLD XCR3064 from Xilinx.

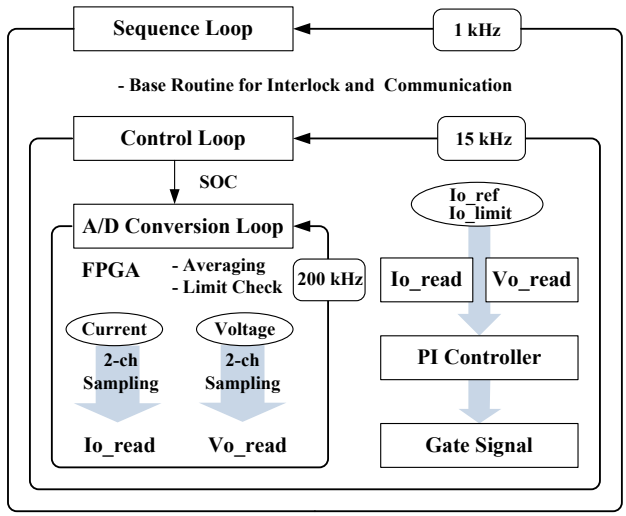

Figure 4: DSP and FPGA program timing assignment.

EXPERIMENTAL RESULTS

The DC link voltage is sixty-six volt which supplies two power stacks in parallel connection. The Fig. 5 shows the load voltage developed on the magnet when output current is 200 A. It is about 36 V with very small ripple voltage which can seem to be ignored.

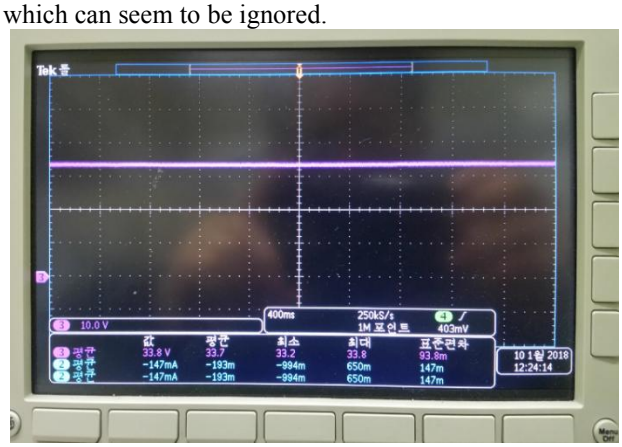

Figure 5: Load voltage developed at the magnet at 200 A.

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The short term stability of the MPS was measured for 60 minutes. The Fig. 6 shows the output current stability of the developed MPS. It showed the 6 ppm-pp at its full output current of 200 A.

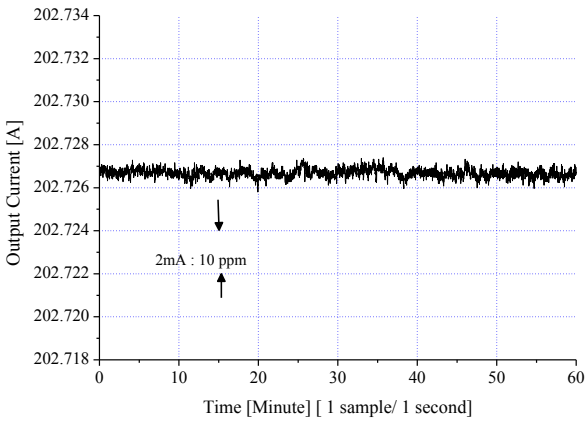

Figure 6: Short term output current stability.

The long term stability for ten hours was also measured. It showed less than 15 ppm-pp as shown in the Fig. 7. If temperature variation was considered, the stability could be reduced to 10 ppm-pp.

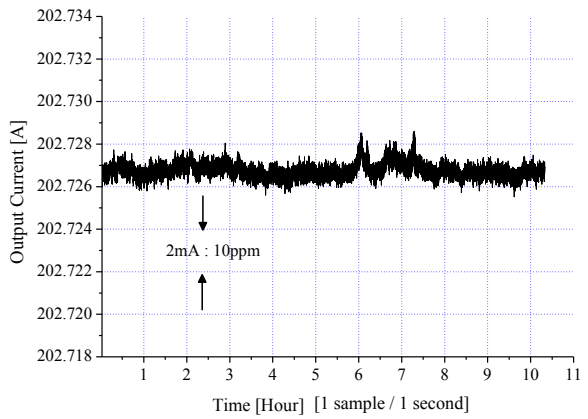

Figure 7: Long term output current stability.

The step responses was tested by the 10 ppm step command at the output current of 180 A as shown in the Fig. 8. It shows less than 5 ppm while repeats several times.

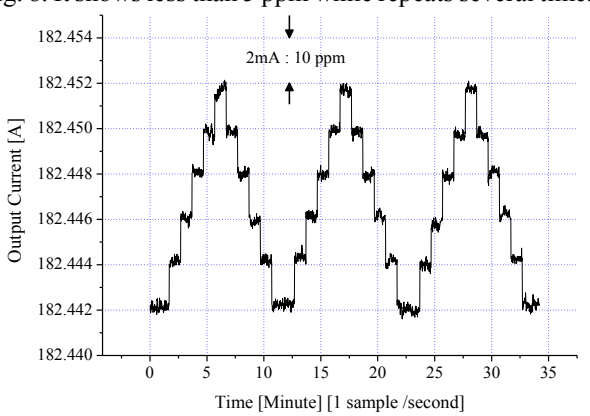

Figure 8: Step responses shows about 5 ppm at output current of 180 A.

Repeatability responses were tested by changing the set current from 170 A to 180A and vice versa several times. It shows about 4 ppm pp as shown in the Fig. 9. The other side of 170 A also shows the same as this value.

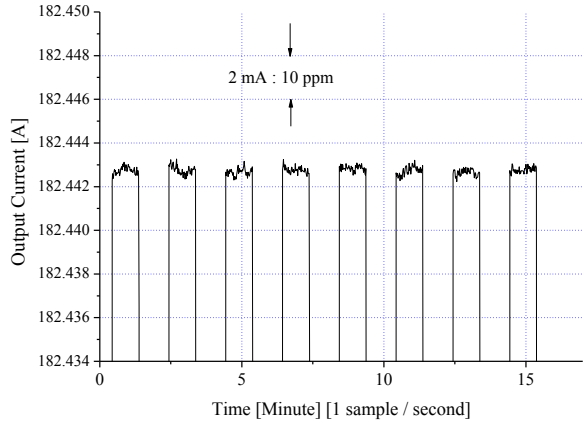

Figure 9: Repeatability test results. This shows about 4 ppm-pp.

CONCLUSIONS

The performance tests of the two ADCs with different resolution were carried out. The ADC which resolution was 16-bit was showed better than that of 18-bit at the same test conditions. It means that the higher resolution of the ADC is not always the best design. It might be depended on the given surrounding circumstances.

The MPS which has output current capability of 200 A was assembled and finished important performance tests. The short term stability for one hour was showed the less than 6 ppm-pp at the output current of 200 A. The long term stability also was very good, which was less than 15 ppm-pp for ten hours at 200 A output current. The step responses showed about 5 ppm-pp with set current command of 10 ppm around 180 A output current. The repeatability test showed within 4 ppm from 170 A to 180 A output current for eight times. The various tests have been going on the developed MPS.

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