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DEVELOPMENT OF NEW LLRF SYSTEM AT THE J-PARC LINAC

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Abstract

In the Low-Level RF (LLRF) system of the J-PARC linac, the digital feedback (DFB) and the digital feedforward (DFF) were adopted to meet the requirement of amplitude and phase stabilities. Almost all modules of the LLRF system were operated without serious problems. However, those for the 324 MHz LLRF system have been used since the beginning of the J-PARC linac and it is concerned about increasing the failure rates. It is difficult to maintain the exact same system because some boards of the present one were discontinued. In addition, the OS and the software to develop FPGA, DSP and the server of this system are too old to be purchased. Therefore, we are starting to study the new LLRF system of the next generation. The digital board of the LLRF system with the Zynq FPGA on the µTCA.4 platform was produced and its basic performance meets the requirement.

INTRODUCTION

In the J-PARC linac, the energy of the beam injected to RCS was upgraded and the front-end was improved to achieve the design power of 1 MW [1, 2].

The twenty-four 324 MHz LLRF systems were installed to accelerate the H^- beam to 191 MeV using RFQ, DTL, and SDTL. The twenty-five 972 MHz LLRF ones were used to drive the ACS cavities of the normal-conducting and the beam is accelerated to 400 MeV for the injection to RCS. These two types of th LLRF system have the functions of DFB and DFF using the Vertex-II FPGA to satisfy the requirement of amplitude and phase stabilities (less than ±1%, less than ±1 deg. at peak-to-peak) [3–5]. However, almost all modules of the 324 MHz LLRF system, which were developed more than ten years ago, have been used since the beginning of the J-PARC linac. Therefore it is concerned about increasing the failure rates.

In the present system of DFB and DFF, the cPCI platform have been adopted and the five modules of cPCI have been used. The three digital modules consist of a FPGA/DSP board, an IO, and a CPU. The two analog ones correspond to a RF&CLK board and a Mixer&IQ-modulator. However, some of the digital boards are already discontinued and the software and the OS to develop FPGA and DSP for this system are too old to be purchased. Table 1 shows the discontinued boards and too old development environment on the LLRF system of the J-PARC linac.

Therefore, we are starting to study the new LLRF system of the next generation.

Table 1: Agenda of the Problems and Too Old Development Environment on the J-PARC LLRF System

FPGA module	discontinued
DSP module	discontinued
CPU module	discontinued, but fungible
FPGA	Xilinx ISE Ver 6.2i
DSP	TI Code Composer Studio Ver 2.1
Host program	Redhat 8.0 gcc compiler Ver 3.2
Application	python2.4, wxPython 2.6

PROTOTYPE BOARD

In the first step, a new digitizer instead of the present three digital modules of cPCI are being developed. The µTCA.4 AMC and RTM is adopted as the platform in the consideration of the future. The feature of this prototype board in Table 2.

Table 2: Feature of the New Prototype Board

platform	µTCA.4 AMC, µTCA.4 RTM
FPGA	Zynq XC7Z045-1FFG900C, QSPI FLASH-ROM 16MB, SD-card Remote Update
RAM	DDR3-SDRAM 1GB×2 (PL, PS)
OS	Xilinx Linux (EPICS-IOC)
ADC	8 ch, 16 bit, 370 MSPS (max.), BW: 800 MHz
DAC	2 ch, 16 bit, 500 MSPS
SFP	2 ports

The AMC board having Zynq FPGA, 16bit-370MSPS ADC, and 16bit-370MSPS DAC is specialized to use the bus of the µTCA.4 standard. The number of ADC becomes eight channels from four of the present system. In addition, two SFPs are mounted for the future expansions and we will be planning to be applied to acquire the all macro-pulse data and to take the J-PARC event-tag.

The RTM board has the PLL and the multiplicity of the clock using VCO. The frequency of the input TTL signal is 48 MHz and the 96 MHz clock to use in FPGA, ADC, and DAC is generated. Whether the clock is inputted from the front panel of the RTM module or from the RF-backplane of µTCA.4 can be selected by the jumper pin. The eight input channels just go through to the µTCA.4 AMC ADCs.

The shelf of µTCA.4 with the bus and the RF-backplane is not used in the first step and the µTCA.4 AMC and RTM are installed to a box with a power supply. The ARM on the Zynq FPGA with linux installed is used as the communication tools instead of a CPU board. Figure 1 shows the block

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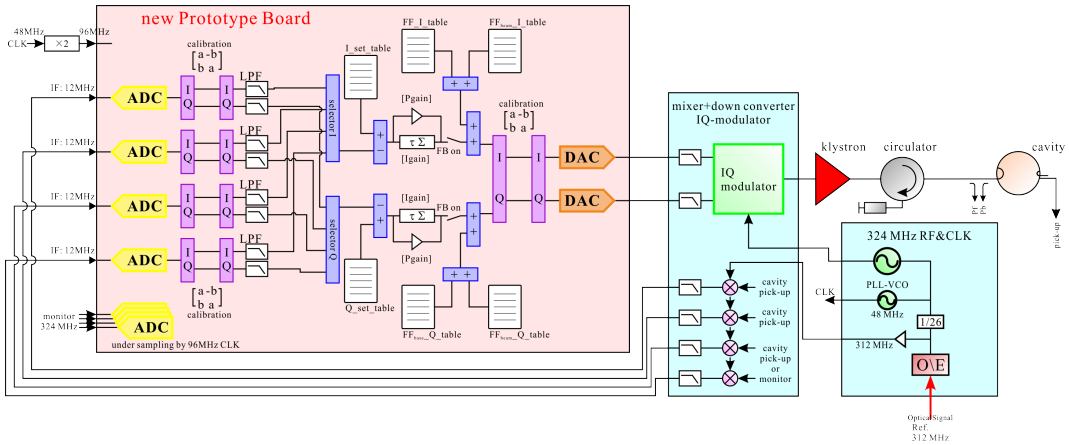

Figure 1: Block diagram of the new prototype board. The red hatching region is the new prototype board, and the modules of the sky blue region, RF&CLK board and mixer&IQ-modulator, of the present cPCI are used in the first step.

diagram of this prototype system. The algorithm of FPGA is almost same as that of the present cPCI system. The IF signals using the present mixer and downconverter are measured by ADC1 to 4 and the 324 MHz RF are monitored using ADC5 to 8 by the direct-sampling.

In the next stage, we would like to develop an analog board of a μTCA.4 RTM.

CROSS-TALK

When the signal was inputted to a certain ADC channel, the separation level of the other channels (cross-talk) was measured as shown in Fig. 2. If a channel of ADC1 to 4 have the 12 MHz RF input signal, the cross-talk was estimated to less than −80 dB in the every channels. On the other hand, the 324 MHz RF signal is inputted to ADC5, 6, and 7[1] which channel is used by direct-sampling method, the −50 dB cross-talk level was obtained in the worst case. It is seen as the cause of the RF characteristic of the zone3 connector between the AMC board and the RTM. However, even in this case, this cross-talk level against ADC1 to 4 using in DFB was less than −80 dB and it is not serious problem.

AMPLITUDE AND PHASE STABILITIES

The stabilities of amplitude and phase in a macro-pulse were measured in the condition using DFB for only ADC1 as shown in Fig. 3. The ADC1 and ADC2 channels using a down-converter and measuring an IF signal were used in the DFB and those stabilities are highly significant. The peak-to-peak values of amplitude and phase in Fig. 3(a) and (b) were archived to ±0.14% and ±0.07 deg., respectively. These results are less than those of the present system and enough to meet our requirement (less than ±1%, less than ±1 deg. at peak-to-peak). In the case of (c) ADC5 using the direct-sampling method and utilized just as a monitor, those were obtained to ±0.37% and ±0.45 deg., respectively.

[1] Since the ADC8 channel was broken, the cross-talk level could not be investigated.

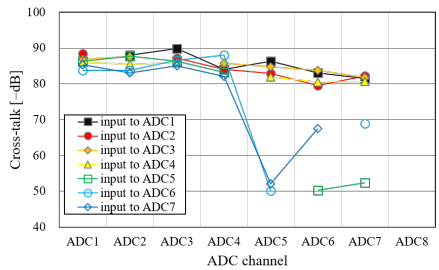

Figure 2: Cross-talk level in the new board. The −50 dB cross-talk level was obtained in the case of the 324 MHz RF signal inputted to ADC5 to 7. However, the ADC1 to 4 channels for the use of DFB were estimated to have the insignificant effect.

Figure 4 shows the frequency components of the ADC amplitudes calculated by fast Fourier transform, FFT. The color lines means the difference of the ADC sampling. There is not an especial spurious and it is a positive result.

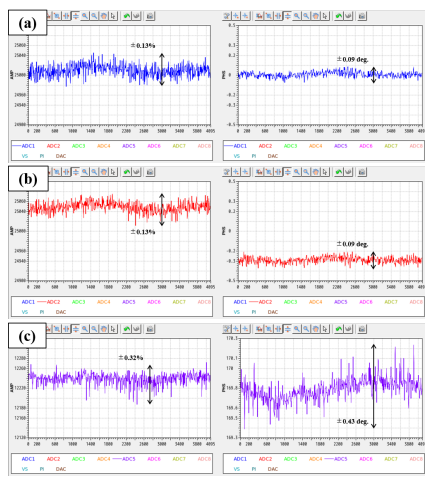

Figure 3: Stabilities of amplitude and phase for (a) ADC1 channel, (b) ADC2, and (c) ADC5 with the condition of DFB using ADC1.

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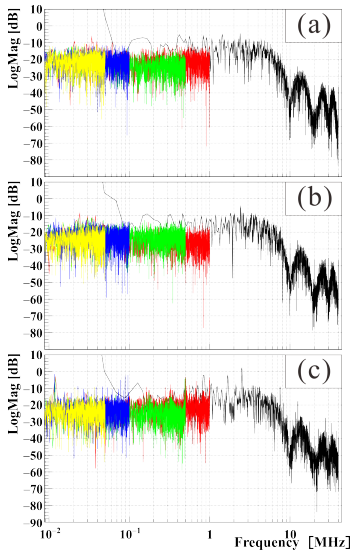

Figure 4: FFT results of (a) ADC1 channel, (b) ADC2, and (c) ADC5 with the condition of DFB using ADC1.

PHASE NOISE

The new RTM board plays a role of the frequency multiplier and generates the 96 MHz clock. Figure 5 shows the phase noises of the 48 MHz input signal and the generated 96 MHz clock measured using the signal source analyzer, Agilent Technologies E5052B. The jitter values of each RF, which are the integral calculation from 10 Hz to 1 MHz, were obtained to 19.4 mdeg. and 26.8 mdeg., respectively. These values were sufficiently smaller than the requirement of the RF clock system (<0.3 deg.).

FUTURE PLAN

The latency of this prototype board was estimated to 1.385 µs. It comes from the high-speed serial communication between ADC and FPGA (JESD204B), which is 1.1875 µs (114 clk at 96 MHz) already after adjusting the elastic buffer. This latency will be causes the increment of the FB-loop delay and decrement of the stability margin. Therefore, the sampling clock will be improved to be 240 MHz from 96 MHz and the latency of the communication process will be reduced to about 0.718 µs.

The beam current of 60 mA will be planned [2] and the beam-loading will be increased. Therefore, we are preparing for the flexible DFF and exploring the possibilities of adaptive DFF [6].

CONCLUSION

In the J-PARC linac, Almost all modules of the LLRF system were operated without serious problems. However, those for the 324 MHz LLRF system have been used since the beginning of the J-PARC linac and it is concerned about increasing the failure rates. We are starting the development of the new digitizer.

The prototype digitizer having the µTCA.4 platform was produced and its performance was estimated. The cross-talk

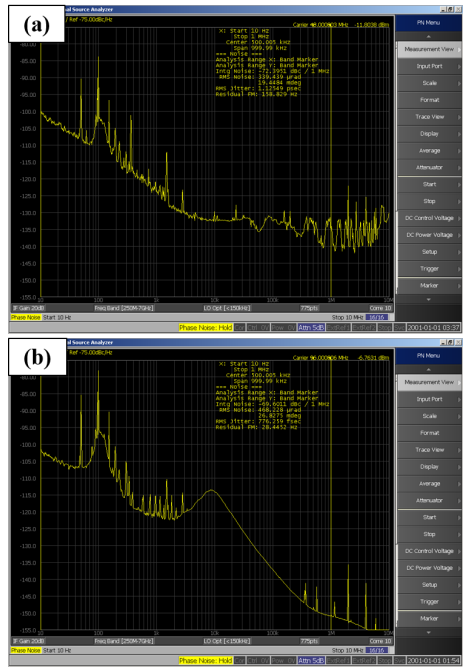

Figure 5: Phase noise of (a) the 48 MHz input signal and (b) the 96 MHz generated clock. The jitter values of the input signal and the clock were obtained to 19.4 mdeg. and 26.8 mdeg., respectively.

level is obtained to less than −80 dB for ADC1 to 4 using for DFB. The peak-to-peak values of amplitude and phase in ADC1 to 4 were archived to ±0.14% and ±0.07 deg., respectively. The phase noises for the 48 MHz input signal and the generated 96 MHz clock were measured and the calculated jitter values were obtained to 19.4 mdeg. and 26.8 mdeg., respectively. These results satisfy our requirement of the LLRF system.

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