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INTERLOCK SYSTEM FOR A MAGNETIC-BEARING PULSE SELECTOR

H. Ishii, J. Adachi, H. Tanaka, T. Kosuge,
High Energy Accelerator Research Organization, Tsukuba, Ibaraki, Japan

Abstract

A new pulse selector with a magnetic bearing has been developed for a hybrid operation mode which has been introduced in the Photon Factory (PF) 2.5 GeV ring of the High Energy Accelerator Research Organization. The pulse selector is used to permit only the passage of an X-ray pulse that comes from the single-bunch part of the hybrid filling pattern. It is mainly comprised of a slit dish-shaped disk fixed at a rotation axis and a motor system synchronized with the radio-frequency signal of the ring. We have adopted a commercially available motor system with a very low jitter of the rotation, which was developed not for a heavy load. The slit disk is so heavy that a rapid deceleration of the rotation can cause a large current to flow back to the motor driver. To avoid the current flow-back problem in the pulse selector system, we have implemented a software interlock and have developed a prototype of a programmable logic controller–based interlock system. The operation of the interlocks in five possible situations has been checked.

INTRODUCTION

A hybrid operation mode has been introduced in the Photon Factory (PF) 2.5 GeV ring of the High Energy Accelerator Research Organization (KEK) [1]. A pulse selector, a type of optical chopper, is used to permit only the passage of an X-ray pulse that comes from the single-bunch part of the hybrid filling pattern. We have developed a new pulse selector which comprises of a magnetic bearing, a dish-shaped and many-slit disk fixed at the rotation axis, a phase-locked-loop (PLL)-controlled motor system, and other parts. The speed and phase of the rotating disk are controlled by transistor-transistor logic (TTL) signals obtained by dividing the radio-frequency (RF) signal of the PF 2.5 GeV ring. A commercially available motor system has been adopted for a sufficiently low jitter of the rotation. The slit disk for the new pulse selector was so heavier than the previous disks in our previous pulse selectors with an air bearing that a rapid deceleration of the rotation can cause a large current to flow back to the motor driver, causing it to fail. An interlock to avoid the current flow-back problem in the pulse selector system is required. We have implemented a software interlock and have developed a prototype of a programmable logic controller (PLC)–based interlock system.

INTERLOCK SYSTEM FOR MAGNETIC-BEARING PULSE SELECTOR

The magnetic-bearing pulse selector system consists of an amplifier module, trigger and clock delay module, pulse-selector controller, magnetic-bearing controller, pulse-selector main body, and interlock system (Fig. 1).

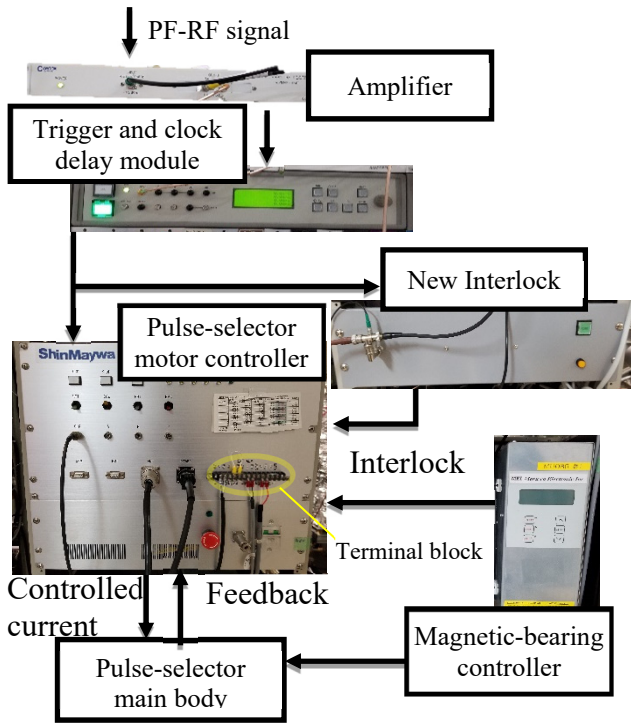

Figure 1: Pulse-selector control system.

The RF signal for the PF 2.5 GeV ring is amplified by the amplifier module and input into the counter circuit. The trigger and clock delay module divides the amplified RF signal into TTL-pulse sequences with a frequency-dividing rate. The TTL-pulse sequence is sent both to the new interlock system and to the pulse-selector motor controller. The pulse-selector motor controller drives the motor of the pulse selector with monitoring encoder. The new interlock system responds according to the TTL-signal frequency to protect the pulse-selector motor controller from the ill effects of the current flow-back.

The pulse-selector motor controller has an emergency button and a terminal block for the external input to protect the equipment. The terminal block is connected to the following three types of interlock.

- Power-off detection
- Detection of magnetic-bearing controller errors
- Newly developed PLC-based interlock system

The slit disk part of the pulse selector is floated by the magnetic bearing and the controller is connected to an uninterruptible power supply (UPS). If a power stoppage to the UPS input is detected, the drive signal of the pulse selector will be cut immediately. The magnetic-bearing controller is connected to the terminal block to signal an error to the motor controller.

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The newly developed PLC-based interlock system is also connected to the terminal block. The trigger and clock delay module is controlled through the simple transmission and retrieval system (STARS) [2,3], which is used as a beamline control system at the KEK-PF. We also developed a software-interlock system with STARS to protect the system from any errors.

A simplified schematic of the pulse selector is shown in Fig. 2. The dish shape, in which the pulse selector revolves, is controlled by the pulse-selector motor controller. The control method is the PLL.

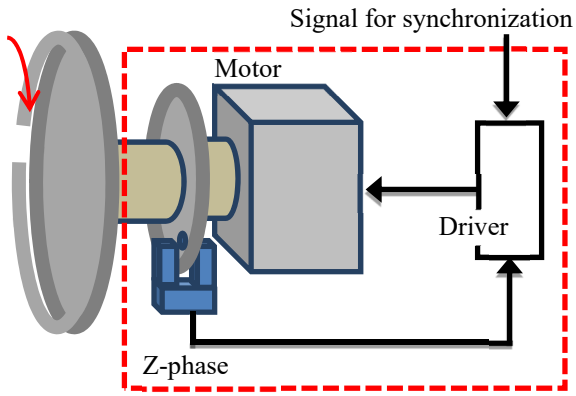

Figure 2: Pulse selector.

Software interlock

The maker of the trigger and clock delay module, Candox Systems Inc., provides a graphical user interface (GUI) to control the module, originally through the Ethernet. The GUI can communicate with the module directly; however, we decided to place STARS between the GUI and the module to log the communications. We also developed a software interlock for this system using STARS (Fig. 3).

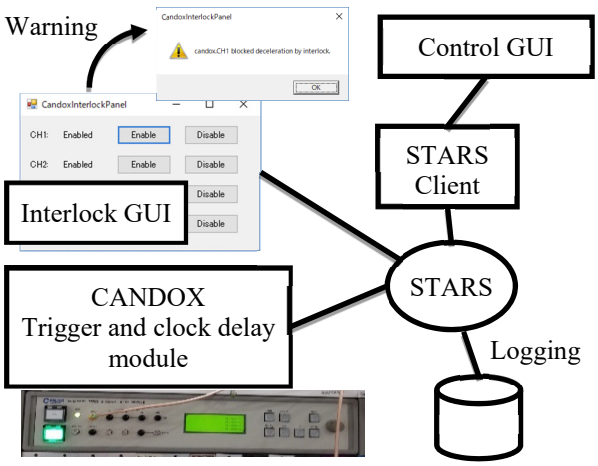

Figure 3: Software interlock system.

When users wish to change the setting of the frequency dividing rate, they must request permission from the interlock GUI. The software interlock system reduces operational errors.

PLC-Based Interlock

The function that detects the frequency deceleration of the TTL signal is implemented in the new PLC-based interlock system. The interlock monitors the frequency of the TTL signal. If it detects a deceleration, the motor-drive signal of the pulse-selector controller is cut. The requirements of the monitoring TTL signal are shown in Table 1.

Table 1: Requirements of the Counter Module

Condition	Value
Sampling interval	10 ms
Input signal type	TTL (3.3 V)
Maximum input frequency	10 kHz

A sufficient sampling-time window is required for monitoring the TTL-signal frequency; however, an overlong time window causes a delay in protecting the pulse-selector controller. We chose 10 ms for the sampling-time window.

The RF signal of PF 2.5 GeV ring (500.1 MHz) is divided by the trigger and clock module, and the module outputs a signal around 10 kHz (maximum). A maximum frequency input of 10 kHz is required for the counter module.

PLC and Hardware

We decided to use a PLC made by OMRON, used widely at the KEK-PF beamline. The PLC-based interlock system consists of the CPU module (CJ2M-CPU13), power module (CJ2M-PA202), DC24V power module for the output (S8VS-06024), counter module (CJ1W-CT021), power relay (MY-4N), a push button, and a lamp (Fig. 4).

The control program was written with Cx-programmer, provided by OMRON for PLC programming. The CPU module stores the count data for the interlock logic program, the configurations, etc. The counter module has frequency inputs and digital inputs and outputs. The power supply module (CJ2M-PA202) supplies DC 24 V to the PLC module and the S8VS-06024 power module supplies DC 24 V to the power relay.

Figure 4: PLC.

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Interlock Logic

Figure 5 shows the flowchart of the interlock logic. When the input RF signal frequency is lower than the minimum value (F_{min}), the interlock system inhibits the motor-drive signal. The minimum input frequency is always renewed. Pushing the reset button resets the interlock system and inputs the minimum frequency. If the RF signal frequency is zero, the interlock cannot be reset.

In the calculation, the input frequency value (f) is copied to the data memory area of the PLC and compared with the minimum frequency value (F_{min}).

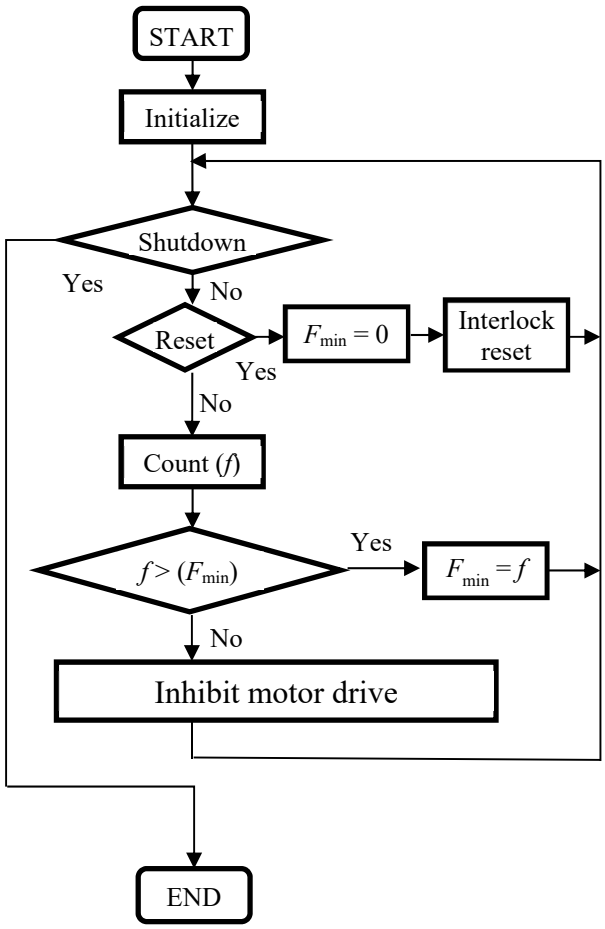

Figure 5: Flowchart of prototype interlock system.

DEVELOPMENT TESTING OF PROTOTYPE INTERLOCK

The prototype of the PLC-based interlock system was implemented and tested with the magnetic-bearing pulse selector (Fig. 6).

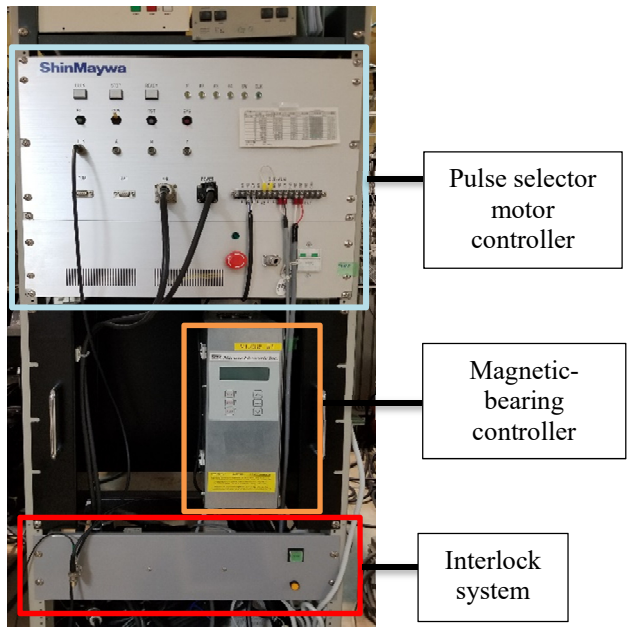

Figure 6: Interlock system and controllers.

The results of the prototype interlock test were as follows:

- When the TTL input-signal frequency rose or was fixed, the motor-drive signal stayed on.
- The motor drive was cut off when the TTL signal frequency fell below the setting value.
- The reset button of the interlock system was disabled without the TTL signal.
- The indicator lamp worked properly in both states (inhibited or enabled) of the interlock system.
- When the TTL input frequency was not zero, the reset button of the interlock system was enabled.

CONCLUSION

We developed a prototype of an interlock system to protect the pulse-selector controller from the current flowback that occurred during the pulse selector's practical use. Input setting mistakes were reduced by the interlock GUI. The motor-drive signal was turned off immediately by the PLC-based interlock system when the TTL-signal frequency decreased. We verified that these interlock systems worked satisfactorily.

The development of a STARS interface for the PLC-based interlock system has been planned, and sufficient functions, e.g., logging, will be implemented.

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