LOW NOISE DIGITIZER DESIGN FOR LCLS-II LLRF*

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ABSTRACT

Modern accelerators use a digital low level RF controller to stabilize the fields in accelerator cavities. The noise in the receiver chain and analog to digital conversion (ADC) for the cavity probe signal is critically important. Within the closed-loop bandwidth, it will eventually become part of the field noise seen by the beam in the accelerator. Above the open-loop cavity bandwidth, feedback processes transfer that noise to the high power drive amplifiers. The LCLS-II project is expected to use an undulator to provide soft X-rays based on a stable electron beam accelerated by a superconducting linac. Project success depends on a low noise, low crosstalk analog to digital conversion. We developed a digitizer board with 8 ADC channels and 2 DAC channels. The broadband phase noise of this board is measured at <-151 dBc/Hz, and the adjacent channel crosstalk is measured at <-80 dB. In this paper we describe the digitizer board design, performance test procedures, and bench-test results.

INTRODUCTION

In the LCLS-II low level RF system design, every half cryomodule (four cavities) use one Precision Receiver Chassis (PRC) and two RF station (RFS) for the field control loop. [1–4] The PRC is the receiver side of the loop and the RFS implement the control algorithm and generate the drive signal. The error signal is transfered from the PRC to the RFS over fiber link in digital domain. In the PRC, we convert four cavity pickup signals and two phase reference line signals. In each RFS, we convert forward, reflected and cavity drive loop back signal from the RF system of two cavities. Including the cavity drive requirements of the RFS, this leads to a requirement for a module with at least six inputs and two outputs.

The digitizer board is carefully tuned to meet specific needs of the LCLS-II LLRF system: the input IF is 20 MHz with an ADC sample rate of 94.3 MS/s, and the output IF is 145 MHz with a DAC sample rate of 188.6 MS/s. All input and output frequencies are coherent. With possible small changes to passive components, the hardware could be used with other frequencies.

We take advantage of the FMC standard for the high speed interface to the digital pins from FPGA. We chose the LPC (low pin count) FMC connector to avoid excessive layer count on the circuit board.

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Besides the core ADC and DAC functions, many small features have been added to the digitizer board to support the specific needs of the LCLS-II LLRF system.

- Synchronous clock to all the ADC and DAC channels, derived from the LO
- Provide an LO/8 signal for up converter
- Electrically compatible with FMC FPGA boards
- SMA connector for analog input and output
- Some GPIO out from FMCs
- Monitor board voltage, current, temperature
- Provide additional slow ADCs and DACs
- Synchronizable switch regulators

DIGITIZER DESIGN

Board Design

The block diagram of the digitizer board is shown in Figure 1, and a picture of the board is shown in Figure 2.

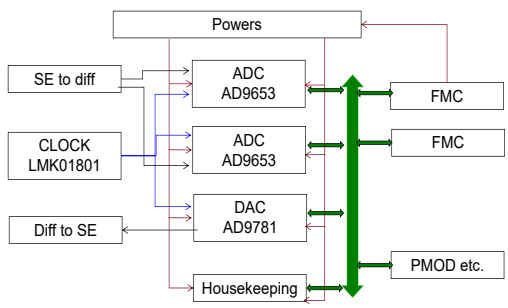

Figure 1: digitizer board hardware modules.

An LMK01801 dual clock divider chip takes the system's LO and divides down to generate the ADC clock, DAC clock, and an offset LO used in the upconversion chain. Bank A is assigned to the ADC/DAC clocks, and Bank B is used for other outputs.

We selected from three modern ADC chips, LTC2174, AD9653 and AD9268, starting by building test boards. [5] During this board development, we evaluated different low-noise regulator configurations for ADC power supplies and reference voltage. We also developed layout sub-pcbs for the modules, and the basic FPGA firmware module for the high speed LVDS serdes.

The AD9563 uses high-speed LVDS lanes like the LTC2174, but has lower noise. Its noise is similar to the AD9268, but its interface uses fewer FMC/FPGA pins.

Both the test boards and the final board are powered by the FPGA carrier board through the FMC connector. The

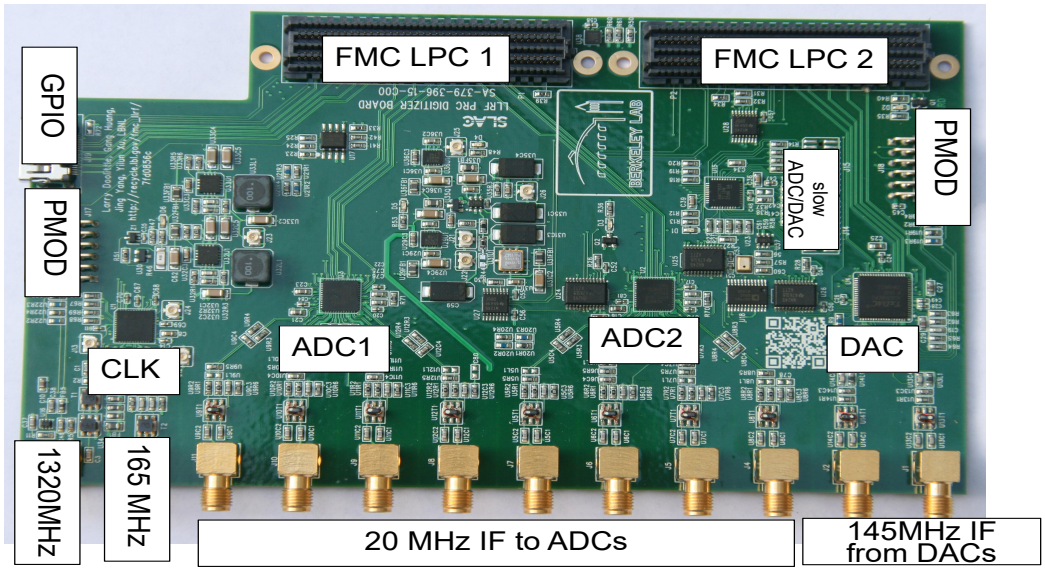

Figure 2: Digitizer Board.

TPS62110 synchronous step-down DC-DC converter is used to provide power to individual LDO regulators. The high precision ADC reference voltage is generated by the low noise and low drift precision reference LT6655. That reference and a discrete Operational Amplifier and transistor circuit provide analog power to the ADC.

IF signals from the downconverter are transformer-coupled to the ADC inputs. To effectively use the clocking resources on the FPGA, LVDS lanes from each ADC should be wired to FPGA pins within the same bank with ADC DCO pins. In our case, with two ADC chips operating at the same frequency, it's good enough to send data to a bank with the other ADC's DCO. This simplified the routing for the board, but added some complexity to the FPGA programming.

The AD9781 DAC is used on the digitizer board, which can provide 2 channel 14 bit DAC output at the relatively high output IF.

The DAC's IF outputs are connected to a band stop filter, and then transformer coupled to the SMA connector for the up converter. The band stop filter suppresses the synthesized spectral line in the first Nyquist zone, 41.6 MHz in this case, leaving the desired line in the second Nyquist zone.

SPI bus interfaces are used to set up the high-speed ADCs, DAC, clock divider and other low-speed features. Pin functions are kept separate, so the low-speed chips can be read out without putting edges on the SPI pins of the low-noise chips.

An AMC7823 from Texas Instruments is used for housekeeping tasks, *e.g.,* monitoring the voltage and current of on-board power supplies and monitor the LO power. Four thermistor bridges for temperature monitoring are read out by an AD7794, a 6 channel 24 bit Σ/Δ ADC.

Each digitizer has a 32 Kbit Serial EEPROM connected on the FMC bus I2C pins, as specified in the FMC standard.

The board layout is on a 8 layer FR4 board. The top layer and two inner layers are used for signal routing. The bottom layer is left flat (except the SMA on the side) to permit conduction cooling. The board use two FMC Low Pin Count connectors for the FPGA side connection, but the board size does not meet the mechanical part of the double wide FMC standard, in part because of the size and pitch of the SMA connectors.

Digitizer Firmware Driver

The digitizer board is only useful when connected to an FPGA, so the FPGA driver development is an essential part of the project. [6, 7] The firmware contains multiple layers of code working together: the chip drivers, the board driver, host computer communication, board test modules, and functional module. A simplified firmware block diagram is shown in Fig. 3.

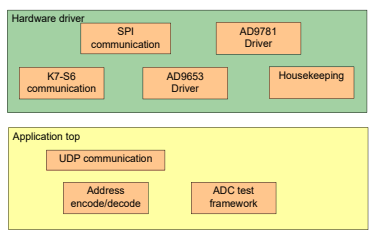

Figure 3: Digitizer FPGA firmware driver modules.

There are chip drivers for the ADC, DAC, frequency divider and other chips on the board. All the FPGA dependencies are encapsulated in this layer.

The board driver is based on the netlist of the hardware design, which means the connection among the modules supporting different chips should be generated according to the connection among the physical chips. [6]

The host communication modules include packet protocol handling and register/memory encoding/decoding.

The working module for the digitizer development is the ADC test framework. [5] As shown in Figure 4, a digital

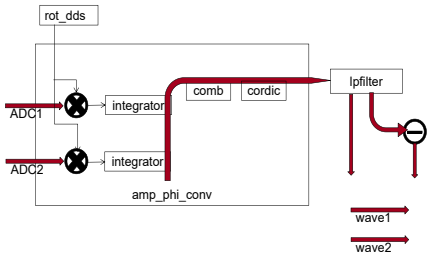

Figure 4: ADC test framework data flow.

local oscillator is mixed with different ADC results, and then passed through a cascaded integrator comb (CIC) filter. The integrator part of the CIC is separated for each channel, while the comb part is decimated into an conveyor belt like data structure. The in phase (I) and quadrature (Q) components are converted to amplitude and phase by a COordinate Rotation DIgital Computer (CORDIC). In order to monitor even longer time scales, an additional low pass filter is used. Waveforms of I/Q and amplitude/phase measurements are passed to circular buffers, to be transferred to the host computer.

Digitizer Software Classes

As part of the digitizer design, we developed Python software to initialize the board and grab data from the FPGA. This is different from the final software for accelerator control, but it contains all the essential components to test the board or use the board. We chose modular design for the software, that corresponds to the hardware configuration. Each chip has its own class, which can be a combination of slow (SPI) signal and/or fast data.

PERFORMANCE TEST

The digitizer board is tested in the lab with a test setup is as shown in Figure 5. The BMB7 is a digital carrier board based on a Xilinx Kintex-7 FPGA, with one FMC LPC and one FMC HPC connector. The LO is generated by a RF signal generator (BNC845), and the IF signal is generated by Agilent 33600A arbitrary waveform generator (AWG). The BNC845 and Agilent 33600A are synchronized by a 10 MHz reference. A spectrum analyzer is used to measure the DAC output.

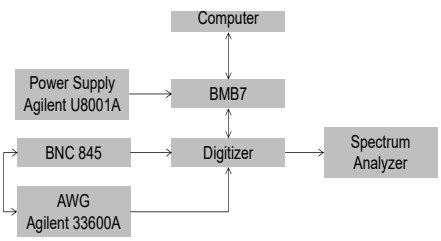

Figure 5: Digitizer bench test setup.

The IF signal from the AWG is split and fed to two digitizer channels, so the two channels share the same LO, power supply, reference voltage and input signal. The measured noise difference represents the noise level of the chip itself. If the two tested channel are two channels on two different chips, then the result will also include the jitter from the clock distribution on the board.

Figure 6 is the measured phase noise density of two channels from the two chips, U3DC *vs.* U2DA. It shows the $1/f$ noise of <-110 dBc/Hz at 1 Hz, and white noise at <-152 dBc/Hz, which meets the requirements of the project.

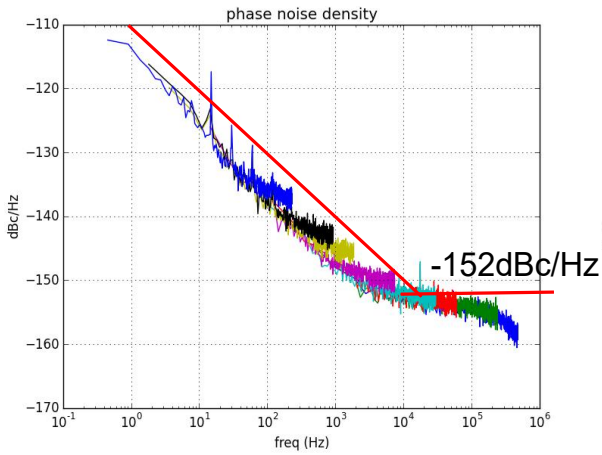

Figure 6: Digitizer phase noise.

CONCLUSION

A circuit board with high performance ADCs and DAC was designed and built for the LCLS-II LLRF project. The phase noise performance exceeds the project requirements. The firmware and software driver are developed as a package together with the hardware design.

REFERENCES

[1] L. Doolittle, A. Ratti, *et al.*, "Design of RF controls for precision CW SRF Light Sources," in *Low Level RF workshop 2013*, Lake Tahoe, CA, October 2013.

[2] L. Doolittle, "Analog-centered LLRF system design for LCLS-II," in *Low Level RF workshop 2015*, Shanghai, China, October 2015.

[3] L. Doolittle and G. Huang, "LLRF Control of high Q_L Cavities for the LCLS-II," in *Proceedings of IPAC2016*, Busan, Korea, 2016.

[4] G. Huang, S.Babel, *et al.*, "High Precision RF Control for the LCLS-II" presented at the NAPAC2016, Chicago, IL, USA, October 2016.

[5] J. Yang and G. Huang, "ADC evaluation boards design and test framework for LCLS-II precision receiver," *Nuclear Science and Techniques*,vol.27 p118, Oct. 2016.

[6] G. Huang, C.Serrano, *et al.*, "Single-source-of-truth coordination of hardware/software development," in *Low Level RF workshop 2013*, Lake Tahoe, CA, October 2013.

[7] G. Huang, L. Doolittle, *et al.*, "Towards beam instrument development system," in *Low Level RF workshop 2015*, Shanghai, China, October 2015.