FPGA CONTROL OF COHERENT PULSE STACKING*

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Abstract

Coherent pulse stacking (CPS) is a new time-domain coherent addition technique that stacks several optical pulses into a single output pulse, enabling high pulse energy from fiber lasers. Due to advantages of precise timing and fast processing, we use an FPGA to process digital signals and do feedback control so as to realize stacking-cavity stabilization. We develop a hardware and firmware design platform to support the coherent pulse stacking application. A firmware bias control module stabilizes the amplitude modulator at the minimum of its transfer function. A cavity control module ensures that each optical cavity is kept at a certain individually-prescribed and stable round-trip phase with 2.5 deg rms phase error.

INTRODUCTION

Investing in advanced kW-class ultrafast lasers will have a very significant impact on particle accelerator systems [1]. However, high pulse energy is achieved at low repetition rate currently [2]. Coherent stacking of several short pulses into a single output pulse in the fiber amplifier system is a promising technique combining high average power and high repetition rate. This Joule-kHz coherent pulse stacking system will revolutionize accelerator applications like LPAs and FELs.

In our experimental coherent pulse stacking system, the oscillator generates a 1064nm optical beam at 400MHz repetition rate with 10 ps pulse width, which is subsequently coupled into a polarization-maintaining single-mode fiber. An amplitude modulator then generates a pulse burst, followed by a phase modulator imprinting the required phase. The first pulses of the tailored optical pulse burst enter the reflecting resonant cavity and interfere destructively at the cavity output port, thus storing optical energy inside the resonant cavity. Later, the final pulse in the burst produces a constructive interference with the previous intra-cavity pulses at the output port, so that all stored energy is extracted from the resonant cavity into a single output pulse [3]. Properly configured sequences of multiple optical cavities will achieve a higher peak-power enhancement factor.

Timing and synchronization are essential for ultrafast pulse addition, and scalable controls are needed for a complex optical system. Here we develop a hardware and firmware design platform to support the coherent pulse stacking application. The ML605 FPGA board processes digital signals captured by high-speed ADC and then sends feedback signals to the modulator and the cavity actuator. A bias control module stabilizes the bias operating point of the modulator while a cavity control module locks the optical cavity phase for pulse stacking. The FPGA outputs the feedback control signal to optical cavities at kHz frequency, to support kHz repetition rates.

HARDWARE INFRASTRUCTURE

The ML605 is an FPGA based digital signal processing board which enables us to create designs targeting the Virtex-6 FPGA. The ML605 addresses the FPGA to commodity-CPU boundary through Gigabit Ethernet and supports GMII (Gigabit Media Independent Interface) from the FPGA to the PHY (physical layer). The FMC110 and the XM105 are added to ML605 through FMC HPC connector and FMC LPC connector respectively.

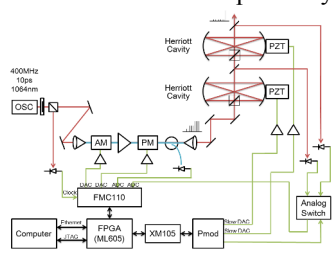

Figure 1: Hardware infrastructure of coherent pulse stacking system.

Figure 1 shows the hardware infrastructure of coherent pulse stacking. The FMC110 is a dual-channel 12-bit A/D (ADS5400) and dual-channel 16-bit D/A (DAC5681Z) FMC daughter card. The sampling clock, which is the master clock signal, is supplied externally by the laser oscillator so as to enable simultaneous sampling at a rate of 400 Msps. A trigger signal at kHz repetition rate, which is derived from the master clock, determines the feedback control frequency (that is the repetition rate described above) and system bandwidth. The XM105 Debug Card is designed to provide a number of multi-position headers and connectors which output FPGA interface signals to slow DACs (which drive the cavity PZTs or modulator bias) and analog switch (which selects signals from multiple photodiodes to one single ADC).

FIRMWARE INFRASTRUCTURE

The FPGA firmware can be divided into three layers: the bottom layer is hardware-dependent drivers, the inter-

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mediate layer is data communication layer, and the top layer is project specific DSP.

The bottom layer is the firmware inherited from FMC110 board hardware dependent drivers. The FMC110 driver design is simplified by relying on proven IP cores. The cores communicate via channels called wormholes.

The intermediate layer is the data structure designed for the FPGA to encode and the host computer to decode. The ML605 communicates with the host computer through Gigabit Ethernet. In the intermediate layer, we configure the PHY to operate in GMII mode. We also develop the data transmission firmware and corresponding software over the UDP-based communication protocol for the ML605 board.

The top layer contains hardware-independent DSP module, the CPS-specific control algorithm and common algorithm implementations. For the data acquired from board to host, the adc_buf (based on the 8to1 dual-ported RAM) is employed to implement the synchronous exchange of high-speed data. To control data from host to board, the dac_buf (based on the 1to8 dual-ported RAM) is adopted to ensure the reliability and rapidity of data transmission. For the slow DAC side, serial data are clocked into AD5628 via spi_master. The bias_ctrl and cavity_ctrl are top level apps to stabilize the bias point and lock the laser cavity phase. We utilize the circular buffer to provide waveforms and register values for upper software layer to display and record.

BIAS CONTROL

For pulse application, it is necessary to control the modulator bias voltage in order to fix the working point at the minimum of its transfer function. Digital control of amplitude modulator bias has been implemented in the feedback loop, so that one can stabilize the operating point of $LiNbO_3$ Mach-Zehnder modulator by varying the bias voltage applied to the DC electrode of the device.

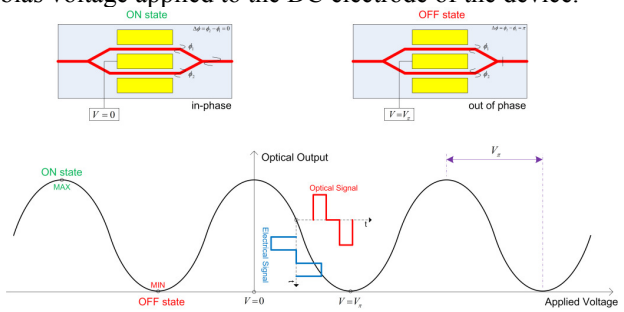

Figure 2: Principle of bias control.

Figure 2 shows the principle of bias control. Bias control module in our feedback loop operates at kHz repetition rate on the FPGA. Three voltages (plus, zero and minus) are added to the modulation signal through the fast DAC while the fast ADC acquires readings corresponding to those voltage steps. The location of the operating point on the transfer function curve is determined by the ADC reading. We vary bias to keep the optical output minimum, where the plus voltage results in a reading that is equal to the minus voltage reading, while the zero voltage reading is the lowest of these three readings. Only proportional control needs to be implemented in the feedback loop to maximize the response speed.

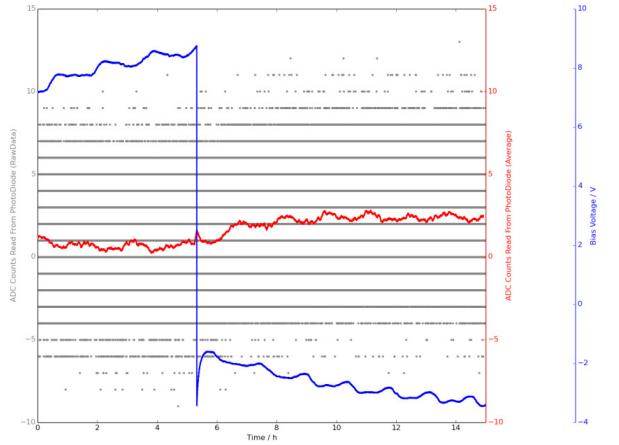

Figure 3: Result of bias control.

Extinction ratio characterizes the modulation efficiency of constructive interference in ON state and destructive interference in OFF state. In our system, extinction ratio of the modulator is 28 dB which suits the bias control requirement. Figure 3 shows that the zero bias point drifts due to temperature. ADC reading from a photodiode maintains a minimal value over 15 hours which means a high extinction ratio, even though there is a steep drop in the bias voltage curve corresponding to a modulo pi reset after a DAC limit was reached.

CAVITY CONTROL

We need to lock the cavity phase at the desired angle in order to realize coherent pulse stacking. A cavity control module programs the slow DAC and drives the PZT to stabilize the optical cavity. From the data flow provided by Figure 4, we can know the digital processing chain of cavity control module.

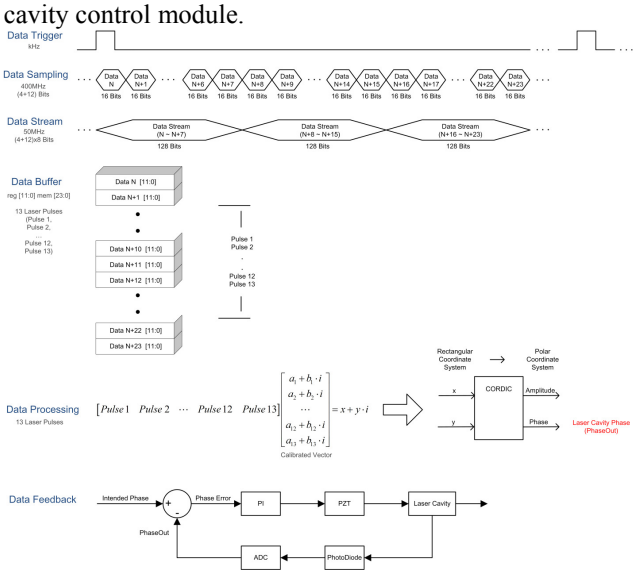

Figure 4: Data flow of cavity control module.

It is necessary to distinguish three different clock domains (400 MHz in sampling clock domain, 50 MHz in processing clock domain and kHz in feedback clock domain) in the system. We know that the time interval of optical pulse is 2.5ns, so the ADC samples the signal directly at 400MHz. Each data stream is composed of 8 consecutive samples, so that the FPGA processes the data at a frequency of 50 MHz. We trigger the feedback control loop at 1kHz. Upon the positive edge of trigger signal, the FPGA records the data sampled by the ADC and starts the feedback control process. We enable a clock counter in firmware to ensure the timing constraints, so the FPGA will finish the feedback loop before the next trigger comes.

We adopt a 13-pulse burst in our optical system. The FPGA buffers the ADC data into a dual-ported RAM whose memory depth is 24. One can adjust the delay to make sure that 13 optical pulses information is captured by the DPRAM. After that, an approximate cavity phase can be computed simply and quickly by a dot-product of the 13-long optical vector measurement with a known complex vector, followed by a rectangular-to-polar (i.e., CORDIC) conversion. The cordicg, a CORDIC processor developed by LBNL in Verilog HDL, is implemented in the FPGA to parse the optical matrix. Once the cavity phase is obtained, PI loop starts driving the PZT to lock the optical cavity at intended phase. Each cavity has its own photodiode to detect the optical pulse signal, however, only one ADC channel is engaged in monitoring these photodiodes. An analog switch is employed to switch the different photodiode channels leading to the single ADC. We alternate in sending the trigger signal to different cavities and do the feedback control for each cavity in turn.

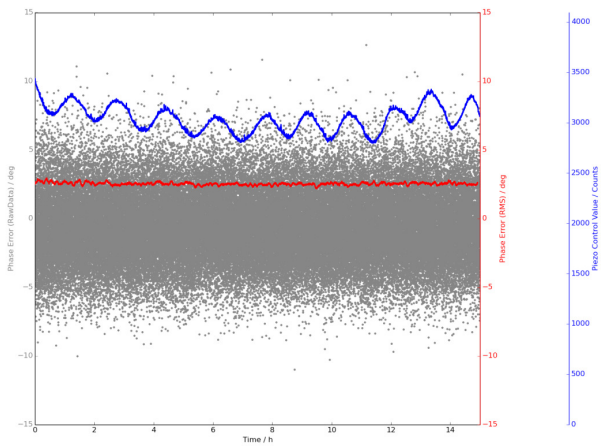

Figure 5: Result of cavity control.

As shown in Figure 5, now we can stabilize two optical cavities simultaneously at target phase using the FPGA over 15 hours, with 2.3 deg rms phase error for the first cavity and 2.5 deg rms phase error for the second cavity. This level of phase stability could ensure an intensity enhancement factor of 7.4 with 13-pulse input [4].

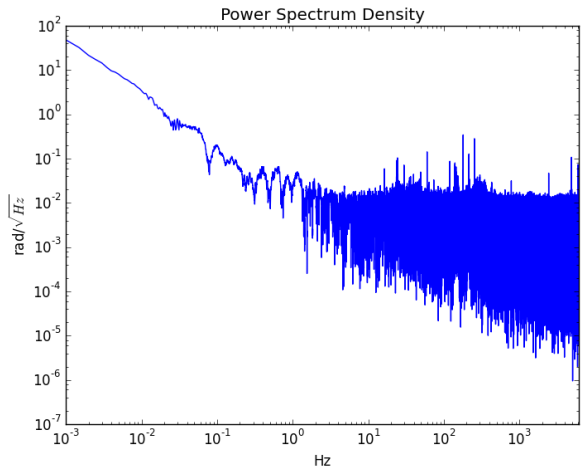

Figure 6: Noise spectrum of cavity phase.

Noise measurements have been made to facilitate the control system design. The noise spectrum could tell us how fast the control loop has to be. Figure 6 shows the Power Spectral Density (PSD) of cavity phase. The cavity phase data are recorded and stored by circular buffer without losing any timing information. We estimate PSD by applying Discrete Fourier Transform (DFT) with Hanning window function due to its low aliasing. The DC average is not usually of interest as a result of the DFT processing, hence we normally remove it from the time series before the FFT is performed. We find peaks mostly locate between 10Hz to 400Hz in the PSD figure. The actuated mirror resonance is the bandwidth limit, however, resonant frequencies (170~400Hz for different mirrors) are OK for now.

CONCLUSION

In conclusion, coherent pulse stacking will overcome limits on achieving energies of short optical pulses from fiber amplifier systems. FPGA enables the coherent pulse stacking system to run at kHz repetition rate under precise timing constrains, and also provides an active cavity-phase control to ensure the stacking-cavity stabilization. Since ML605, FMC110, XM105 are all readily available commercial boards, and the firmware is separated into different independent layers, it is feasible to expand the hardware and firmware platform to accommodate a cascade of multiple resonant cavities.

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