INTEGRATED CONTROL SYSTEM FOR AN X-BAND-BASED LASER-COMPTON X-RAY SOURCE [*]

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Abstract

LLNL's compact, tunable, laser-Compton x-ray source has been built around an advanced X-band photogun and accelerator sections and two independent laser systems. In support of this source, the control system has developed into an integrated architecture that continues to grow to simplify operation of the system and to meet new needs of this research capability. In addition to a PLC-based machine protection component, a custom, LabView-based suite of control software monitors systems including low level and high power RF, vacuum, magnets, and beam imaging cameras. This system includes a comprehensive operator interface, automated arc detection and rf processing to optimize rf conditioning of the high-gradient structures, and automated quad-scan-based emittance measurements to explore the beam tuning parameter space. The latest upgrade to the system includes a switch from real-time OS to FPGA-based low-level RF generation and arc detection. This offloads processing effort from the main processor allowing for arbitrary expansion of the monitored points. It also allows the possibility of responding to arcs before the pulse is complete.

INTRODUCTION

A compact laser-Compton x-ray source based on x-band accelerator hardware has recently been commissioned at LLNL [1]. While the accelerator was being built and brought online, a remote control system was developed in parallel to run it, with features added on demand as the accelerator grew in complexity and as tasks amenable to automation became apparent. For this control system, National Instruments LabView was chosen as the basis for the bulk of the control system, with PLC logic supplementing it to provide basic IO and machine protection functionality. Other platforms, such as EPICS, were considered but not selected as they generally have a steeper entry curve getting the first devices online with no local experience. Using LabView, basic functionality was able to be provided rapidly. Also, given the relatively small scale of the system, the highly distributed nature of EPICS was unnecessary. Once the platform was chosen and the software grew in complexity, there has not been a need to reconsider that path.

In this paper, we present an overview of the key components of the control system: the RF control chassis, the machine protection system (specifically with regards to breakdown damage), and the auxiliary support system controls.

RF SOURCE

Low level RF control, and all RF monitoring, is performed using a National Instruments (NI) PXI system running the real-time version of LabView. User interface is provided by a comprehensive front panel that communicates with the real time controller through a mix of shared variables and network streams. Figure 1 gives the detailed clocking diagram driving the accelerator system. The master timing reference is an MXO-PLMX from Wenzel Associates, which relies on an 11.9 MHz reference oscillator coupled with a low noise frequency multiplier that provides a 2.586 GHz master clock. This 2.586 GHz signal is used by the MenloSystems electronics to phase-lock the 81.6 MHz oscillator to the RF clock and generate a synchronized 10 Hz trigger.

Low-level RF Pulse Generation

The master clock is multiplied by a factor of 4 to provide the 11.424 GHz X-band RF used in the accelerator. This RF signal is then modulated via an IQ mixer with greater than 100 MHz of bandwidth. The I & Q ports are driven by an Active Technologies AT-1212 2-channel, 14-bit arbitrary function generator (AFG) connected to an NI PXI-7954R Flex-RIO board. Performance of this system is detailed in Ref. [2]. Currently, a simple square pulse is generated, but once a planned RF pulse compressor is installed, more complicated shaping (such as a phase flip in the signal) will be easily implementable. This shaped pulse is supplied to the traveling wave tube and klystron for amplification to ~50 MW.

Modulator Control

The klystron is powered by a Scandinova K2-3X modulator, providing 420 kV, 330 A pulses. The modulator is equipped with it's own manufacturer-supplied control hardware and software, which provides network-based access to all necessary controls and readbacks. This system also controls the klystron solenoid magnets and monitors water flow through the system. The relay-logic based facility personnel safety system ties directly into the modulator, preventing the high-voltage circuits from being energized without a permissive signal supplied by the facility.

A custom interface screen was created in LabView to simplify operator interaction with the modulator and avoid having to manually adjust operating parameters, such as the cathode filament current, each time the system was turned on and off. This also allows the built-in LabView datalogging capabilities to monitor the performance of the modulator and keep a log of beam operating time.

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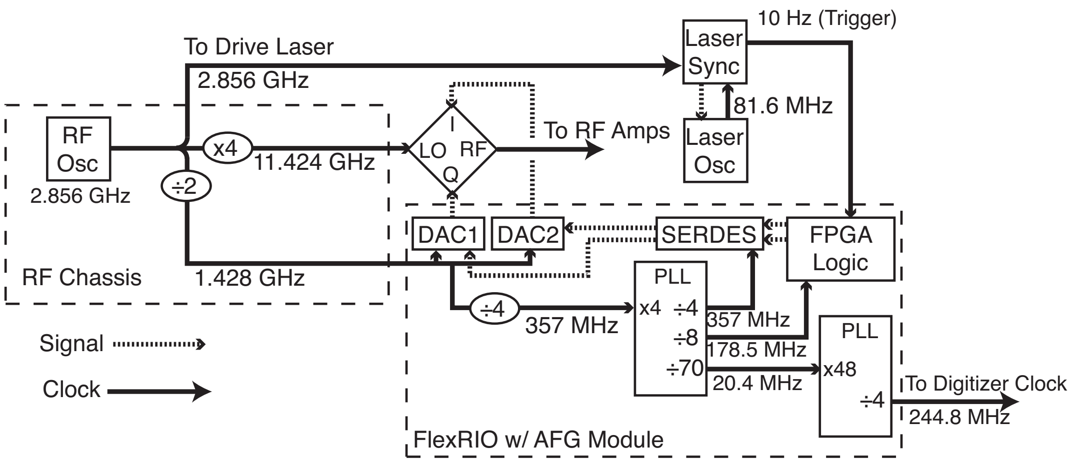

Figure 1: Diagram of the low-level RF pulse generation system and clock logic.

ARC DETECTION

Both during conditioning and for routine operations, it is important to monitor the system for signs of breakdown in the waveguide and accelerating structures. To accomplish this, we have developed an automated arc detection and recovery system. This system is currently being transitioned between two architectures.

High-speed Digitizer Arc Detection

RF power detector diodes monitor transmitted and reflected RF power at the klystron output, the photogun input, and the section input. These signals, along with signals from the integrating current transformer and other diagnostics, are fed to a bank of 1 GHz, 8-Bit Digitizers (NI PXI-5154) in the RF control chassis. These traces are available to the user at a rate that depends on the network connection to the interface panel and the other processes on the interface machine; we typically get 1-3 Hz refresh rates for routine monitoring. Based on user configurable parameters, summary data is also presented, such as klystron, gun, and section power, gun gradient, and current charge.

Although not every trace is transmitted to the front end, each of the channels is checked on every shot for signs that an arc occurred, and the system can store all the traces locally for later retrieval and analysis. Based on user specifications at the interface panel, arc could be detected as either the trace exceeding some trip level within a gated window or the integral of the difference between two consecutive shots exceeding some threshold level. If any channel shows either of these conditions, the chassis inhibits firing of the modulator and low-level RF pulses and alerts the user. In manual mode, the user can adjust the power level, clear the arc error, and resume operations. During conditioning however, generally an “autoramp” mode is used, where the operator configures a waiting period, then a series of ramp speeds to slowly, but automatically, bring the power back up to the breakdown gradient. The system monitors this progress and switches back to manual mode if arcing starts occurring at lower and lower gradients, indicating a problem that needs operator attention.

FPGA Arc Detection

We have recently demonstrated similar arc detection functionality in an FPGA-based system. Using NI 5761 4-channel, 14-bit, 250 MHz sample rate digitizers connected to an NI PXI-7954R FlexRIO module, both the limit and difference integral functions can be evaluated as the data arrives, allowing for a system response on the time scale of tens of nanoseconds, rather than the milliseconds required to complete a trace, transfer it to the processor, analyze it, and transmit and execute the reaction commands. Since the processing doesn’t require the collection of a complete trace, this system can also run at an arbitrary rep rate, even for continuous beams. This architecture also offloads almost all the processing effort from the control processor, allowing easy expansion to a very large number of channels with negligable decrease in performance.

The trigger input to the FPGA hardware is limited to the resolution of the 250 MHz system clock. If the incoming signal has no phase relationship to the FPGA clock, a single-tick jitter is virtually certain. Figure 2 gives an example. When we are running at 60 Hz, the Greenfield 9404 PXI timing card internal trigger has no defined phase relationship to the digitizer clock, and so a significant (1 tick) jitter is seen. However, when we are using the 10 Hz provided by the sychronized laser system, the jitter drops significantly.

This jitter becomes an issue during the difference integral measurement. Even with two identical traces, the integral can vary due to noise at the bit level. If the pulses aren’t exactly lined up on the sample clock, the calculated difference integral can grow much higher. This requires us to set the threshold higher than we otherwise would, to avoid frequent false-positives, and results in occasionally missing small arcs (based on observed vacuum presure spikes). To correct for this, a simple step is to check the integral for the three cases of aligned traces and traces off-by-1 in each direction and report out the lowest value. This is straightforward to

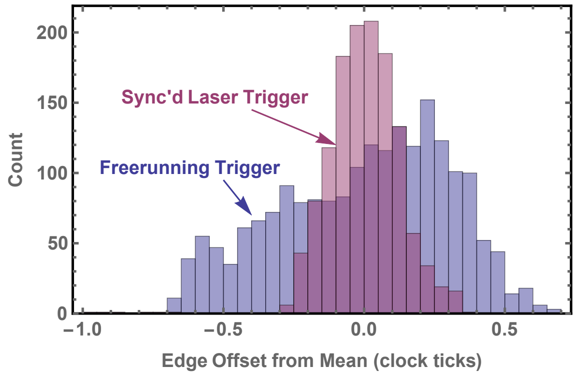

Figure 2: Effect of trigger stability on measured FPGA digitizer trace. A synchronized trigger result in more stable pluse measurement.

implement in the FPGA hardware, and Fig. 3 shows the result. The peak reported integral value drops by nearly half for the unsynchronized data, allowing a much lower alarm threshold to be reliably established. A synchronized signal still yields better performance, but not significantly due to the long tail shown.

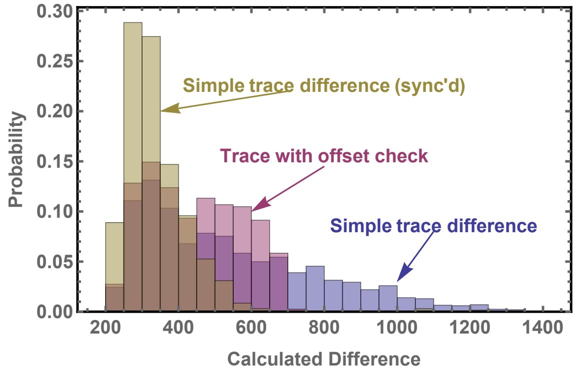

Figure 3: Effect of trigger stability and calculation method on distribution of measured integrals.

We have implemented this architecture for a single channel so far, and plan to roll it out for all the channels once testing is complete.

AUXILIARY SYSTEMS

Most of the remaining systems that require operator control are based on self-regulating hardware that provides command-based control via some form of serial or network connection. Serial devices, using either RS-232 or RS-485 standards, are connected to NI serial-to-ethernet adapter boxes, allowing all devices to be accessable from any machine.

In most cases, a "back end" control program deals with the direct communication with the devices, and provides access points, via shared variables, in the LabView environment. This allows multiple front end programs to access the controls (for example, both the main control screen and the automated quad-scan program can control the same quadrupole magnet). For the magnet power supplies, ion pumps, and Gigabit ethernet cameras, all of which have many devices to communicate with, the system was designed to allow the addition of new devices without having to change the basic code, merely to update the configuration with information about the new device, minimizing the need to recompile and redeploy the software as additional supplies came online as the machine grew. These systems rely on LabView's actor framework to spin up a control channel for each physical communication channel (one for each network or RS-232 device, and one for each RS-485 bus which might have multiple addresses), periodically poll the devices, and report out the current status, as well as respond to commands to change the parameters. Again, because the shared variable architecture is being used, the built-in logging capability can be leveraged to monitor and search for long-term trends in the machine operation.

Smaller scale systems (such as the chillers stabilizing the gun, section, and solenoid temperatures; the stepper motors controlling the RF power distribution and phase and diagnostic positioning; or the digital delay generators providing system timing) have simpler architectures that are hand-built to talk to a specific set of devices. However, since the code is well developed from the systems mentioned above, it's likely that these systems will be moved to the expandable architecture the next time one needs to be updated.

CONCLUSION

Routine accelerator operation and x-ray experiments rely on the stability of the control system described here. The architecture has been designed to be easily expandable to add new components or new functionality with minimal disruption. The next developmental step will be to roll out the complete FPGA architecture for the arc detection and upgrade the timing system to allow synchronized triggering at repetition rates other than 10 Hz, to allow better performance during conditioning operations, followed by the activation of the RF pulse compressor and controls.

REFERENCES

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[2] D. J. Gibson, R. A. Marsh, G. G. Anderson, C. P. J. Barty, "Compact X-band Accelerator Controls for a Laser-Compton X-Ray Source," in *Proc. IPAC'16*, Busan, Korea, May 2016, `doi:10.18429/JACoW-IPAC2016-THPOW027`.