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NSLS-II INJECT LINAC RF CONTROL ELECTRONICS UPGRADE*

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Abstract

The electron injection LINAC of NSLS-II Synchrotron Light Source is designed to operate in both single-bunch and multi-bunch beam mode (MBM). In the MBM operation, the beam bunch train length varies from 40 to 150 bunches which translates a beam loading time of 80~300ns in time. That requires that the LINAC rf control front-end module (FE RFM) have a sufficient control bandwidth (estimated 100 MHz min.) to be able to effectively perform the necessary adaptive feed forward control (AFF) for the beam loading compensation. The RFM from the LINAC OEM has successfully supported the commissioning and the operation to the date. However, the issues in its performance, reliability and support pose the need to develop an upgraded rf control in-house to better support NSLS-II operation. The RFM electronics upgrade is designed with the emphasis on meeting the specific operation needs of NSLS-II injector LINAC, and the capability of being best integrated in the existing accelerator control infrastructure. The implementation strategy is to use the modern digital rf components and designs to achieve the best result, while leveraging the built-in digital radio IP to minimize the amount of required IP development effort, and thus reduce the development costs and risk.

NSLS-II INJECTOR LINAC OVERVIEW

NSLS-II LINAC is a 2.998MHz, 200MeV Pre-Injector to the following Booster Synchrotron which in turn serves as the injector to the final Storage Ring. It delivers minimum 0.5nC of charge in Single-Bunch Mode, and up to 15 nC in Multi-Bunch Mode (or MBM). The length of an MBM varies from 40 to 150 beam bunches, or 80~300nS in time. The basic parameters are listed in the Table 1 below. The LINAC rf chain starts with the rf modulating grid PA for a YU-171 Electron Gun, followed by a 500MHz Sub-Harmonic Buncher, a 3GHz Pre-Buncher and a Final Buncher as the LINAC Front-end, and a following four traveling-wave structure LINAC powered by two 45MW klystrons to bring the beam energy to the required 200 MeV [1].

RF TRANSMITTER DOWN-STREAM PA'S

The NSLS-II LINAC down-stream RF power plant is shown in the system diagram in Fig. 1. In the LINAC front-end, a 500MHz/2.5kW Solid-State RF Power Amplifiers (or SSA) is used to drive the Electron Gun modulating grid (500MHz/500W) for MBM beam, a 500MHz/500W SSA to drive the Sub-Harmonic Buncher; and a 3GHz/1.2kW SSA to drive the Pre-Buncher (PB, 3GHz, 1.2kW). The following 3GHz, 4-section LINAC is rf-powered with three 45MW klystrons (Toshiba E37302A). The two klystron stations in position #1 and 3 are needed in the normal operation, while the Klystron in Station #2 is in standby and can be switched in to back up Klystron #1 or # 3 should either one fail.

The high-performance, compact solid-state switching modulators that support the klystrons are a commercial product. The details about these SS switching modulators are reported in a companion paper [2]. The rf drives for the rf PA and klystrons are provided by the rf modulator front-end, its electronics and functions are described in the following section.

Table 1: NSLS-II LINAC Parameters

Nominal energy	200 MeV
Minimum Energy with single klystron failure	170 MeV
Repetition rate f_{rep}	from single shot to 10Hz
Geometric Emittance, $4\sigma x \sigma x'$	150 nm-rad at 200 MeV
Energy spread $\Delta E/E$	< 0.5% rms
Pulse to pulse energy jitter	< 0.2% rms
Pulse to pulse time jitter	< 50 ps rms
Short pulse mode	
Length of a single bunch at 500 MHz repetition rate	< 330 ps
Time structure	1 single bunch to bunch trains with separation between consecutive bunches of 2 to 10 ns.
Maximum charge per bunch Q_b	> 0.5 nC
Relative bunch purity before and after pulse	< 1%
Long pulse mode	
Pulse train length	160 – 300 ns
Corresponding number of bunches at 500 MHz repetition rate	80 – 150
Maximum charge per pulse train	15 nC
Relative charge difference between bunches in the pulse	< 10%

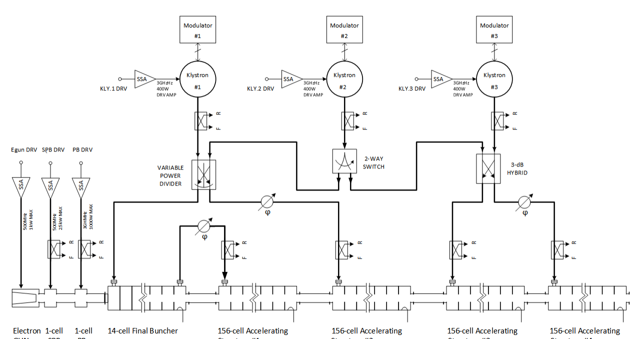

Figure 1: The NSLS-II LINAC rf power plants are comprised of three Solid-State RF PA's for the beam bunchers in the front-end and three 45MW klystrons for the following 4-section 3GHz accelerating structures.

RF MODULATOR FRONT-END

The LINAC rf control front-end electronics is a digital rf modulator (RFM). Its first primary function is to performs the phase and amplitude control of the rf drive to the down-stream high-power rf plants. The second primary function of the RFM is the beam-loading compensation in MBM operation to order to keep the beam energy dispersion within the tolerance over the beam bunch train.

In the 500MHz sub-harmonic buncher, the beam-loading effect shows up on both the phase and amplitude of the buncher cavity field, while the effect is only on the rf amplitude in the following 3GHz LINAC section.

The magnitude of the effect gradually grows over the beam bunch train, and the cavity field is consequently distorted. To counteract this cavity field distortion by the

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beam-loading, a time-varying rf vector pattern is added in the RFM rf drive output waveform as a mean of feed-forward control (FF), and to maintain the cavity field constant with the presence of the beam. The MATLAB simulation plots in Fig. 2 illustrate the beam loading and compensation effect in the scenario of the sub-harmonic buncher where the beam rf vector is basically perpendicular to the vector of cavity field.

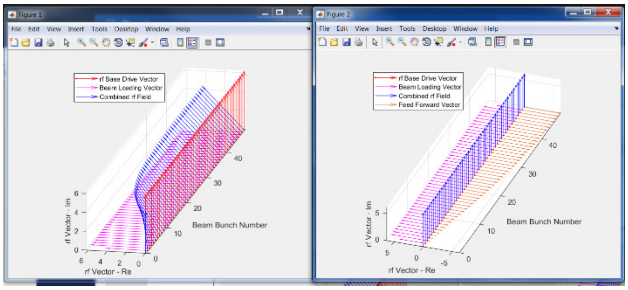

Figure 2: Beam-loading effect of Multi-Bunch beam in the rf field (left) and its compensation with Digital Pre-Distortion (or "feed-forward") rf modulation (Right).

PROCESSOR-NODE BASED RFM NETWORK ARCHITECTURE

The subject of the optimum accelerator control system architecture with distributed microprocessor-node networks was studied by the experts in the accelerator labs as early as in mid-80's [3, 4]. Over three decades, a lot more of high-performance processor/controller/DSP devices have become widely available at relatively low-costs, and that has made the implementations of the envisioned processor-node based control network architectures even easier with many more options.

For NSLS-II LINAC, total six RFM's are needed to individually and digitally control the rf of eGUN modulating grid, Sub-harmonic Buncher (SHB), Pre-Buncher (PB), and the klystron station #1, 2, and 3. Each RFM is a self-contained computer node with the standard Ethernet port (GigE) for the connection to the accelerator control Ethernet, and the Event Receiver port (EVR) to receive the timing codes from the timing distribution fibers. It also has the necessary rf sampling ADC/DAC channels for interfacing with RF I/O signals which will be further discussed in more details in the following section.

All six RFM nodes are connected to a single network switch under a dedicated area server computer to form a private subnet to insure the data communication between the six RFM's and the server. The EPICS I/OC also runs on this server for the high-level control tasks. The architecture of the LINAC RFM control network is shown in Fig. 3.

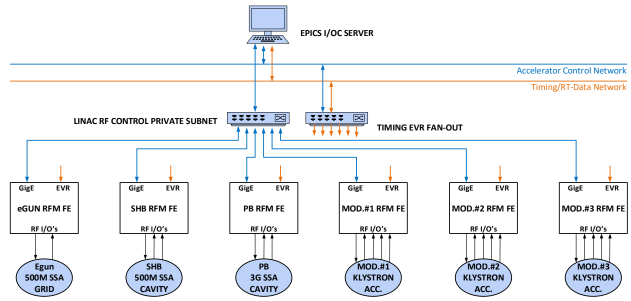

Figure 3: All LINAC RFM nodes are networked in a private subnet within the global control network.

RFM NODE HARDWARE

The digital RFM is designed to be a self-contained, stand-alone computer node in the accelerator control network. Hardware-wise, it is very much like the Digital Radio path in a cellular communication base-station [5] comprised of the following major function blocks and I/O interfaces as indicated in the block diagram in Fig. 4.

- Digital RF transmitter upstream implemented with an ultra-speed Tx_DAC's to generate the rf carrier for the down-stream rf PA (SSA or klystrons), and the baseband data input and the internal DSP of the Tx_DAC performs the Digital Pre-Distortion (PDP) modulation as the Feed-Forward Control for the beam-loading compensation.
- Multi-channel DPD Observation digital receiver implemented with the ultra-high speed direct rf sampling Rx_ADC's to measure and monitor the rf signals at various points of the transmitter rf path as well as the rf field in the associated accelerating cavity/structure.
- GigE network connection with a TCP Offload Engine (or TOE).
- Embedded Timing Event Receiver (or EVR) in FPGA to facilitate the required synchronous operation of each RFM in the rf system.

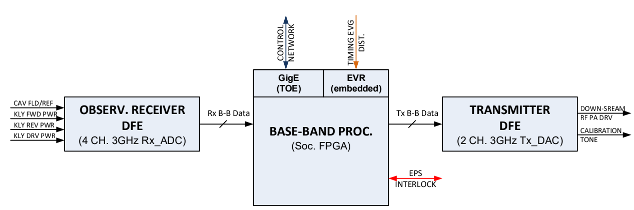

Figure 4: The RFM hardware design is primarily a digital radio (with both Tx and Rx) supported by the interfaces for the control Ethernet and the Timing Event Receiver.

DIGITAL RF DEVICE EVALUATION

Among many suitable ultra-speed Tx_DAC's, the 16-bit, 12 GSPS RF DAC/DDS AD9164 is being evaluated for the transmitter path of the RFM radio. With the AD9164 running at 6GHz clock rate in Mixed output mode, the 3GHz/500MHz carrier frequency can be directly, digitally synthesized with a decent -73dB SNR in the close-in region as shown in Fig. 5. The baseband modulation data rate is set to 500MSPS with a data interpolation of 12 to keep the data rate at a reasonable rate while ensuring a 200MHz+

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DPD modulation bandwidth for having an effective compensation for the beam-loading.

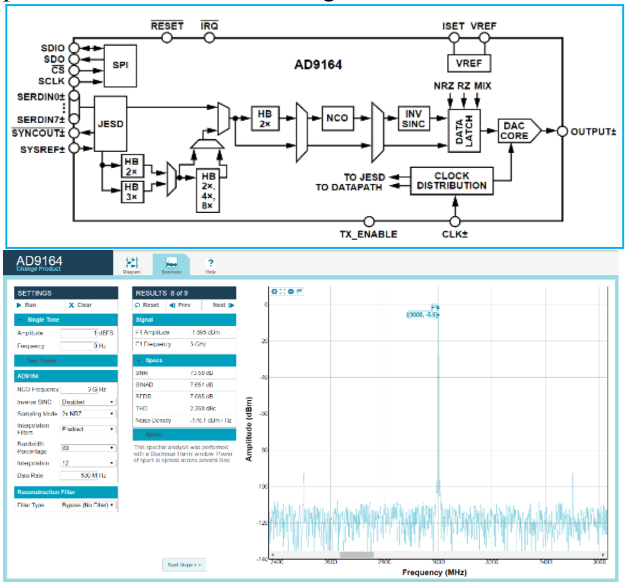

Figure 5: Output spectrum and SNR of AD9164 Tx_DAC directly synthesizing a 3GHz transmitter carrier frequency with a 6GHz clock and 500MSPS baseband data input.

For the 4-channel DPD observation receiver path of the RFM radio, the direct rf-sampling Rx_ADC AD 9689 is being evaluated. With AD9689, the 3GHz rf signals are first directly sampled at the quadrature-sampling rate of 2.4 GSPS to demodulate the 3GHz rf to the 600MHz IF data stream, then the internal 600MHz NCO and DDC with a factor of 8 decimation rate further demodulate the IF to a reasonable 300 MSPS baseband data rate with a 62dB SNR (Fig. 6).

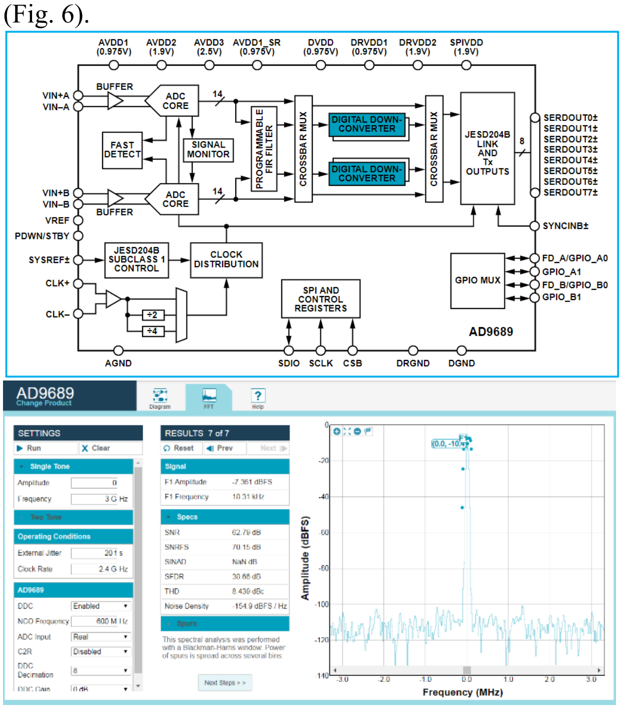

Figure 6: AD9689 Rx_ADC SNR performance evaluated at 3GHz for the RFM DPD Observation receiver application.

CONCLUSIONS

The existing RF control electronics from the LINAC OEM successfully supported the commissioning and has been supporting the rf operation to the date. Its performance, reliability, and lack of necessary testability has created the need for an upgrade.

The RFM-node network architecture for the NSLS-II LINAC area RF control upgrade is based on the research on the optimum accelerator control system designs conducted in national accelerator laboratories. It improves the control system performance and streamlines the data processing. In the RFM hardware design, the goal is to achieve the best performance while keeping the development costs and risk to minimum, and the strategy is to leverage the state-of-art hardware/firmware IP's that telecommunication industry offers in their off-the-shelf ASIC devices. The R&D is being actively pursuit in the NSLS-II RF Group, and the various technology for the implementation is under evaluation. The progress will be reported in future publication.

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