ISBN: 978-3-95450-223-3 ISSN: 2673-7000 doi:10.18429/JACoW-NAPAC2019-TUPLM29

CURRENT STATUS AND PROSPECTS OF FRIB MACHINE PROTECTION SYSTEM*

Z. Li†, D. Chabot, S. Cogan, S.M. Lidia
Facility for Rare Isotope Beams, East Lansing, Michigan, USA

Abstract

The Facility for Rare Isotope Beams (FRIB) is designed to accelerate beam up to 400 kW power with kinetic energy ≥ 200 MeV/u. Fast response of the machine protection system is critical for FRIB beam commissioning and operation to prevent damage to equipment. The beam commissioning of the first LINAC segment, including fifteen cryomodules, has been completed. Four ion species were accelerated to a beam energy of 20.3 MeV/u with duty factors from 0.05 percent to continuous wave. The peak beam current exceeded 10 percent of the final requirements. This paper summarizes the status of the machine protection system deployed in the production, Machine interlock response time of ~8 μs was achieved. Incentives for future development include being able to achieve smooth and reliable beam operation, faster machine protection response time and real time data analysis of failure mode.

INTRODUCTION

The Facility for Rare Isotope Beams (FRIB) is designed to accelerate beam up to 400 kW power with kinetic energy ≥ 200 MeV/u. Fast response of the machine protection system is critical for FRIB beam commissioning and operation to prevent damage to equipment. The beam commissioning of the first LINAC segment (LS1), including fifteen cryomodules, has been completed. Four ion species were accelerated to a beam energy of 20.3 MeV/u with duty factors from 0.05 percent to continuous wave. The peak beam current exceeded 10 percent of the final requirements [1]. Room temperature and cryogenic button-style BPMs, AC current transformers (ACCTs), halo monitor rings, fast thermometry sensors on the cryomodule beam pipe, scintillator-based neutron monitors for beam loss detection, LLRF controllers and PLCs of front end, LS1 and its folder section are connects to MPS [2].

The machine protection system safeguards the cryomodules and ensures that beam will be tripped off in case of any fault and violation of presetting beam parameters. During the beam commissioning, from the ACCT network detecting a fault of over-power or power-loss-over-threshold conditions, or from fast events detected by the LLRF controllers, to the moment when beam is inhibited, the response time of MPS is within 35 μs [1, 2]. This paper will focus on MPS system structure and its FPGA logics currently implemented in the production line for LS1 commissioning and discussion of its future improvements.

*Work supported the U.S. Dept. of Energy Office of Science under Cooperative Agreement DE-SC0000661.
†liz@frib.msu.edu

MPS CURRENT IMPLEMENTATION

FRIB MPS is built with master and slave structure [2], where slave nodes collect OK/NOK status from MPS sensor devices [2] and pass to the master through optical fibre daisy chain which uses Time-division multiplexing technique to carry sensor information of each slave node. MPS master processes the information of each sensor received and also the machine status of its own to decide the operation state. It requires 33 slave nodes and 6 master-slave daisy chains to fully cover FRIB front end and LS1 area for machine protection. Since the MPS master can only handle two daisy chains due to limitation of FGPDB [2] board, displayed in Figure 1, a "reptile" structure of MPS was deployed in the production line where we have multiple master nodes consisting of "head", "body" and "tail". Each master node can hold 2 daisy chains with maximum of 16 slave nodes. Master nodes communicate with each other the operation states through RS422 serial state links and also are connected to the EPICS IOC through individual Ethernet cables to be able to configure mask bits [2] of sensor devices simultaneously. Master FPGA logics is designed such that only the master head can accept the EPICS process variable (PV) command to change the operation state. The rest can synchronize their operation states to master head through RS422 links in μs scale and broadcast the synchronized operation state to each slave node on their daisy chains. Each master node can make the decision to enter fault state based on its sensor inputs and machine status and lock up the rest nodes through a dedicate fault link.

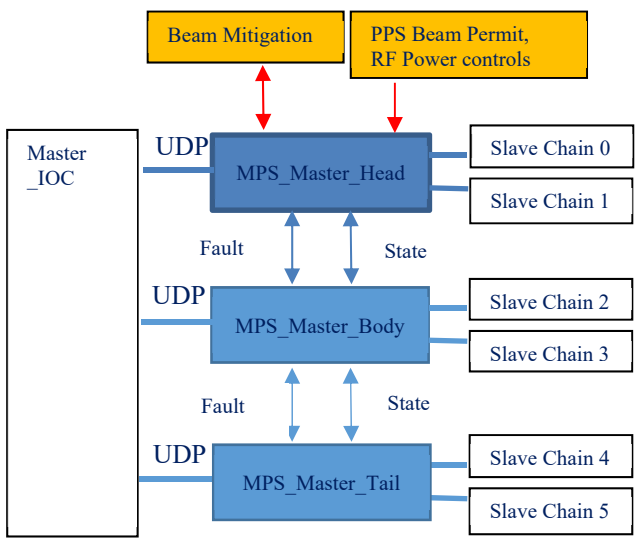

Figure 1: MPS of reptile structure deployed in production.

ISBN: 978-3-95450-223-3 ISSN: 2673-7000 doi:10.18429/JACoW-NAPAC2019-TUPLM29

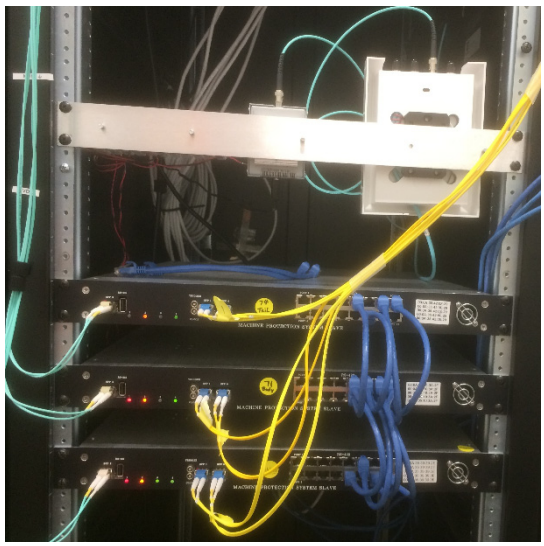

Figure 2: MPS master head, body and tail in the production line.

One advantage of such a "reptile" structure MPS is that it can grow as many daisy chains as user needs by adding additional body sections. Another advantage is that each section (master or slave node) of this "creature" is controlled by a FPGA and it can decide a fail-safe mode in case communication to master head is lost. A picture of such structure MPS masters in the production is displayed in Figure 2.

The final decision of beam mitigation is made by MPS master head. Master head listens to each enabled MPS sensor from the entire MPS network and trips off the beam in case of sensor NOK (not OK) and informs LLRF to turn off RF cavities in case of PPS NOK through slave nodes. All MPS master and slave nodes run with state machine which provides a reliable and steady control to mitigation devices as well as to LLRFs.

MPS master state machine has 5 operation states. As displayed in Figure 3, these are MPS fault, disable, monitor, enable [2] and PPS fault. PPS fault state are recently added for RF cavity protection. LLRF controller is required to turn off RF drive in case of a PPS event which results in AC power to the RF amplifiers being removed. The RF amplifiers can be damaged if LLRF continues to drive RF with that the transistor drain voltage is already too low while the DC power supplies are decaying, and then a cavity discharges into the amplifiers that can result in negative

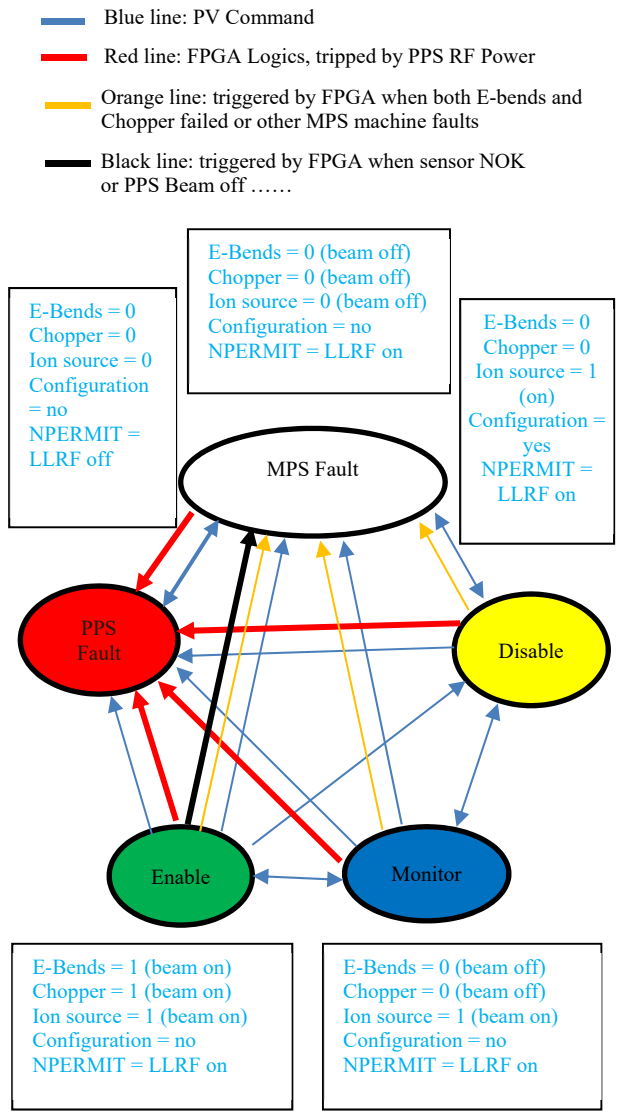

Figure 3: MPS master operation state diagram. Highlighted in blue line, Master head can listen to the PV commands to change the operation states, the rest master nodes can only accept the commands from the head through the state link. Highlighted in red line, each master node will enter PPS fault state at PPS event. Highlighted in yellow and black line, each master node can decide to enter fault state based on the inputs from MPS sensor devices, machine status of MPS. Each master node can broadcast its fault state to the entire MPS network though fault links and daisy chains.

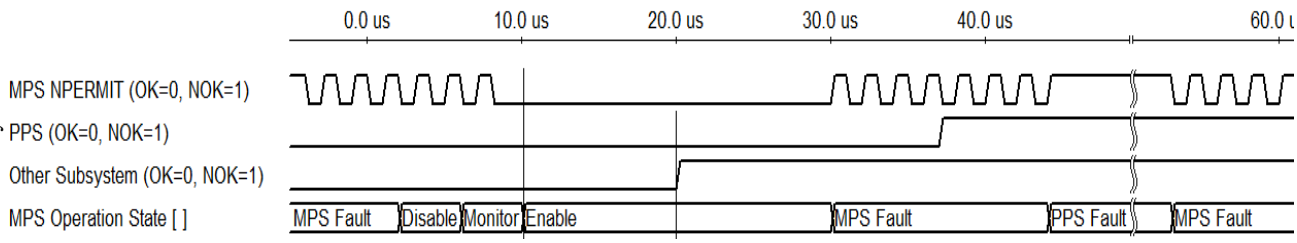

Figure 4: NPERMIT signal vs. MPS operation state. MPS moves into MPS fault state from enable state when subsystem is NOK and then to PPS fault state when PPS is NOK, NPERMIT signal is changed from steady 0 to 1 μs pulse and then steady 1 signal.

ISBN: 978-3-95450-223-3 ISSN: 2673-7000 doi:10.18429/JACoW-NAPAC2019-TUPLM29

drain voltage. This requires MPS to provide a NPERMIT signal which is through a RS422 connection to LLRF such that LLRF controller can distinguish between a regular NPERMIT, which tells if MPS is enabled, and the NPERMIT caused by PPS Fault, which tells RF cavity needs to be power off. As displayed in Figure 4, when MPS master is at enable state, the NPERMIT to LLRF is steady 0 which informs LLRF the circular buffer of post mortem data shall start to run, if MPS is moved out from enable state to any state other than PPS fault, NPERMIT will become 1 µs pulse which notifies LLRF that beam is turned off and circular buffer for post-mortem data shall be frozen but leave RF power on. NPERMIT is steady 1 signal in case of PPS fault state. In such a way MPS can inform LLRF of PPS event within 10 µs which provides enough time to turn off the RF cavity before power supplies decay (~10 ms).

As we can see from Figure 3, a machine fault of MPS itself can trigger a fault state; one such machine fault can be the MPS response time error. A series of pipelined counters with 8ns clock cycle time are implemented in FPGA logics to count the response time from each query of master to the response received from each individual slave on the chain, a machine fault will be generated and fault state will be triggered if it exceeds ~10 µs.

TEST IN THE BEAM LINE

The MPS response time measurement has done with ACCT [1] and chopper monitor [3] in the LS1 commissioning and the result is within design expectation of 35 µs. Also, 116 LLRFs currently installed in the production line are tested the response time with an automated test program, the worst case scenario is within 10 µs from the moment that LLRF sends out NOK to that MPS master head latches the fault and activates the mitigation devices; another test of worst case response time is for PPS event and its test result is within 2 µs from the moment that MPS master sends out NPERMIT signal of PPS event to that LLRF receives the signal and reacts. Also, all PLCs which monitor front end area and cryomodules and 13 MicroCTAs (diagnostic devices) connected to MPS are tested to trip MPS successfully with forced NOK signals.

CONCLUSION AND FUTURE PROSPECT

The MPS with 6 daisy chains and 33 slave nodes which connects diagnostic devices, LLRFs and PLCs in the area of the front end and LS1 has passed the LS1 commissioning and its machine protection response time is within 35 µs. Currently a reptile structure with multiple master nodes are implemented in the production because of FGPDB hardware limitation. A proposal is made to use latest Xilinx Zynq FPGA to host embedded IOC with its Petalinux kernel plus Debian file system and to combine multiple master nodes into one Zynq FPGA board. A prototype of embedded IOC has been successfully developed on ZC706 board which can control the GPIO ports through EPICS PVs. Therefore the future MPS system with advanced FPGA technologies will be much fast and reliable in terms of EPICS control, response time, post modem data acquisition, fault pattern tracking and analysis.

REFERENCES

[1] J. Wei *et al.*, "The FRIB SC-Linac - Installation and Phased Commissioning," in *Proc. 19th Int. Conf. RF Superconductivity (SRF'19)*, Dresden, Germany, Jun.-Jul. 2019, paper MOFAA3.

[2] Z. Li, L. R. Dalesio, M. Ikegami, S. M. Lidia, L. Wang, and S. Zhao, "FRIB Fast Machine Protection System: Engineering for Distributed Fault Monitoring System and Light Speed Response," in *Proc. 28th Linear Accelerator Conf. (LINAC'16)*, East Lansing, MI, USA, Sep. 2016, pp. 959-961. doi:10.18429/JACoW-LINAC2016-THPLR046

[3] Z. Li, D. Chabot, S. Cogan, S. M. Lidia, and R. C. Webber, "FRIB Fast Machine Protection System: Chopper Monitor System Design," in *Proc. 29th Linear Accelerator Conf. (LINAC'18)*, Beijing, China, Sep. 2018, pp. 336-338. doi:10.18429/JACoW-LINAC2018-TUPO007