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EVALUATION OF THE XILINX RFSoC FOR ACCELERATOR APPLICATIONS

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Abstract

As electronic technology has evolved, accelerator system functions (e.g. beam instrumentation, RF cavity field control, etc.) are increasingly performed in the digital domain by sampling, digitizing, processing digitally, and converting back to the analog domain as needed. A typical system utilizes analog to digital (ADC) and digital to analog (DAC) converters with intervening digital logic in a field programmable gate array (FPGA) for digital processing. For applications (BPMs, LLRF, etc.) requiring very high bandwidths and sampling rates, the design of the electronics is challenging. Silicon technology has advanced to the state where the ADC and DAC can be implemented into the same device as the FPGA. Xilinx, Inc. has released a multi-GHz sample rate RF System on Chip (RFSoC) device. It presents many advantages for implementing accelerator and particle detector systems. Because direct conversion is possible, RF analog front/back end and overall system design is simplified. This paper presents the results of an evaluation study of the RFSoC device for accelerator and detector work, including test results. It then discusses possible applications and work done at SLAC.

INTRODUCTION AND MOTIVATION

Many applications in particle accelerators [1,2] and detectors involve the sampling of an analog signal, conversion to a digital quantity, processing in the digital domain, presentation of the processed measurement (e.g. beam position data), and in some cases, conversion back to the analog domain to drive an actuator. The architecture of such systems is very similar in many instances.

Figure 1 shows the block diagram of a generic accelerator instrumentation and/or control system with digital processing. It should be noted that important differences may exist in the analog front- and back-ends as well as the required system sampling rates. The implementation of such a system has traditionally involved using discrete ADC and DAC components tied to an FPGA. With the hardware interconnects between components involving many parallel wires, or in more modern high-speed devices, medium to very high-speed serial data paths utilizing such interface standards as JESD204B [3]. The disadvantage of this configuration is the added hardware for supporting electronics in the ADC & DAC (power supply, clocking, auxiliary SPI control interfaces, etc) as well as the firmware complexity in the ADC/DAC digital interfaces. All of which, in turn, drives up power consumption, increases board space and ultimately system cost and reliability. For systems requiring many processing channels, these costs can be prohibitive.

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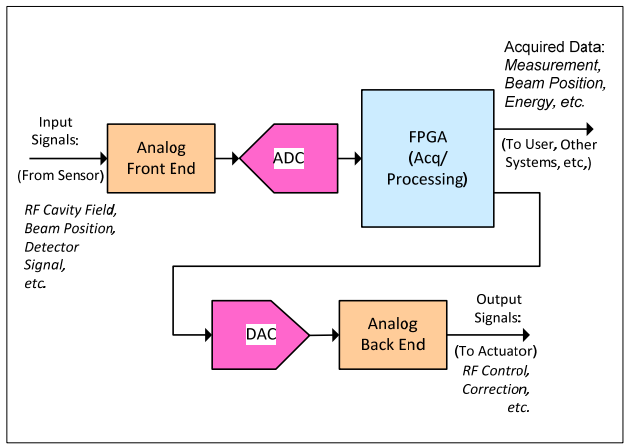

Figure 1: Generic control/instrumentation system.

With the introduction of the RFSoC device, the size, power consumption and hardware complexity issues are reduced to the point where it makes this device becomes an attractive candidate for certain accelerator applications. Added advantages include simplified RF front and back end design (via direct conversion at higher BW and sampling rates) and reduced system latency, which is critical for feedback applications.

THE XILINX RFSOC

The Xilinx RFSoC device [4], part of its Zync System On Chip product line, integrates multiple channels of high-speed ADCs and DACs onto the same silicon as the FPGA fabric. The fabric itself contains digital logic elements, static RAM blocks and DSP Multiply-Accumulate (MAC) units. Added to this are many peripherals including multi-core ARM CPUs, DDR4 memory interface, high-speed SERDES blocks (for Ethernet, PCIe, etc.). A block diagram [5] of the RFSoC is shown in Fig. 2.

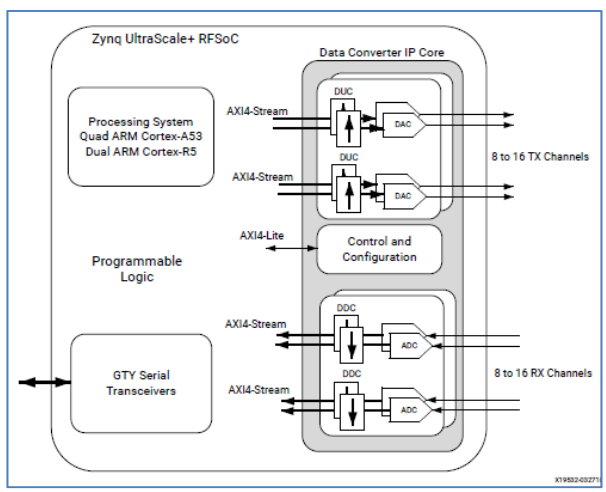

Figure 2: RFSoC device block diagram [5].

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The RFSoC device is built on a 16nm CMOS silicon process, utilizing FinFET technology [6]. This product was developed targeting 5G network base stations which require many channels with high bandwidth. Thus the device architecture and choice of peripherals reflects this.

Focusing on the data converter sections, the device contains eight 4GSa/s (or 16 2GSa/s) 12-bit ADCs and eight (or 16) 6GSa/s 14-bit DACs. The number of ADCs/DACs varies between components in the device family. Newer generations in the product line increase the converter sampling rates up to a maximum of 5GSa/s and 10GSa/s for the ADC and DAC, respectively. Note that two ADC channels are interleaved to obtain the 4GSa/s rate. The ADC if followed by a complex Digital Down Converter block (complex mixer, NCO, decimation filter); the DAC has a complementary Digital Up Converter in front of it for additional signal processing. These blocks can be bypassed if not needed. The ADC is built upon an interleaved architecture of 500MSa/s 14-bit successive approximation subconverters. Thus, active calibration is utilized to remove interleaving spurs [6].

DEVICE EVALUATION

In order to determine the viability of this device for applications in accelerator systems, we performed a series of measurements to verify that the device performed as well as the datasheet claims in terms of noise and dynamic range. In addition, some additional tests were performed focusing on device performance in terms of many tones.

The device manufacturer provides an evaluation board (model ZCU111) along with a reference firmware design and software to exercise all of the device features. This evaluation package we used to perform our measurement studies. The evaluation system software provides for output of ADC data into LabVIEW (.lvm) text data file format and input of DAC data in the same format. This enables the user to develop offline analysis and generation tools using Matlab.

The measurements performed in our studies where: dynamic performance (AC performance) via single- and two-tone DAC and ADC measurements. These types of measurements give good indication of converter performance [7,8] parameters such as Spur-Free Dynamic Range (SFDR), Noise Spectral Density (NSD) and Equivalent Number Of Bits (ENOB). It is these parameters that we focus on in selecting devices for typical applications. Other parameters (e.g. SNR, SINAD) are of interest, but are not highlighted here.

Measurements were first performed on the DAC, then the ADC. For two- and multi-tone tests, the DAC itself was used as a signal source for the ADC after it was verified to perform satisfactorily.

DAC Measurements

DAC performance was measured using a high-performance spectrum analyser (Agilent E4440A PSA) and an adjustable bandpass (K&L Microwave 5BT series) filter at the DAC output tuned to the frequency of interest. DAC tone signal data was generated using a custom Matlab application with care taken in the selection of tone frequencies to ensure coherent sampling [7]. Measurements were take over a range of tone frequencies spanning 124…3000 MHz, with the DAC sampling rate running at 6389.76MHz. The SFDR, NSD, IM2 and IM3 parameters are measured from the spectrum analyser. A summary of DAC single and two tone measurements at three frequencies is shown in table 1.

Table 1: DAC Measurement Results

Test Frequency (MHz)	One-Tone SFDR (dB)	One-Tone NSD (dB/Hz)	Two-Tone IM2 (dB)	Two-Tone IM3 (dB)	Two-Tone NSD (dB/Hz)
240	67.76	-152.8	-62.95	-67.21	-152.7
765	62.54	-153.3	-62.54	-69.57	-153.3
1900	67.98	-153.6	-64.60	-75.01	-152.6

These measurements and those performed at additional frequencies are in close agreement with those of the device datasheet [9]. Note that the NSD figures are limited by the noise floor of the spectrum analyser, which was measured to be -153dBm/Hz.

Additional testing applied a comb of 2000 tones out of the DAC spanning low (10MHz) frequency up to 2 GHz with a spacing of 2MHz. This test was performed for a Multiple Input Multiple Output signal processing application where Intermodulation Distortion (IMD) performance becomes critical due to distortion product mixing of the large amount of signals present. A plot of the DAC output on the spectrum analyser with this signalling profile is shown in Fig 3.

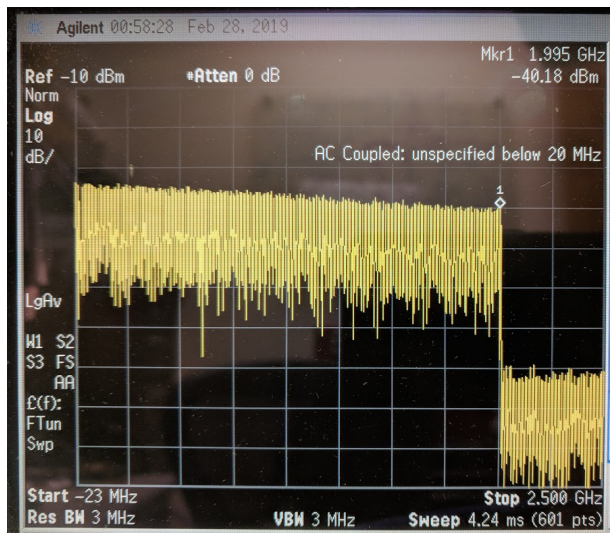

Figure 3: 2000 tone DAC output.

The sinx/x rolloff of the DAC is visible in the gentle slope across the spectrum. Noise spectral density was measured to be -102.3dBc/Hz. It is worth noting that the tone frequency spacing was slightly randomized to ensure a non-integer frequency relationship between tones, which can lead to a cancellation between IMD products causing an unrealistic lowering of the noise floor.

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ADC Measurements

For ADC testing, a high spectral purity RF synthesizer (Agilent E4432B ESG), followed by a bandpass filter was used for single-tone testing. Two- and multi-tone testing used the DAC as a signal source. ADC data was acquired using the evaluation board software and saved into LabVIEW formatted ASCII data files. Due to the nature of the reference firmware design the ADC record length is limited to 65536 samples because of the FIFO length chosen.

Custom Matlab code was written to translate the LVM formatted data and perform signal analysis on a selected data file. The time-domain data is transformed into the frequency domain where signal analysis is performed, extracting the previously mentioned performance parameters. The ADC was tested in single- and two-tone configurations over the range spanning 100MHz to 3GHz (above Nyquist), with a sampling rate of 4.096GHz. Table 2 shows performance results for single-tone tests for a selected set of frequencies.

Table 2: ADC Single-Tone Test Results

Test Frequency (MHz)	SFDR (dB)	NSD (dB/Hz)	ENOB (bits)
240	73.92	-150.94	9.29
765	68.59	-149.95	9.09
1900	67.02	-144.95	8.27

The measured performance agrees closely with the values specified in the datasheet. An FFT plot, generated by our custom Matlab ADC analysis tool, is shown in Fig. 4.

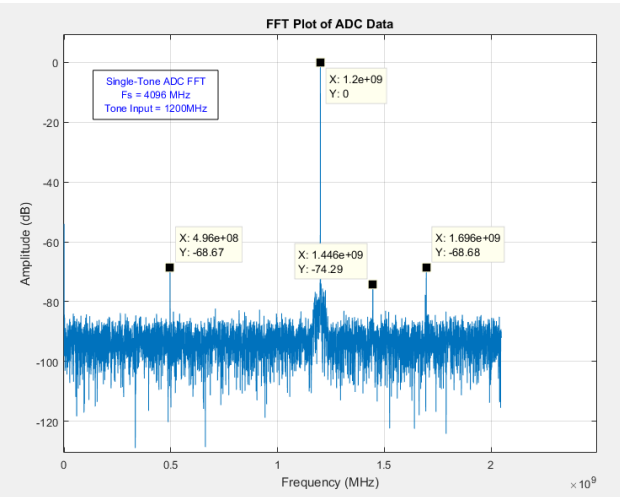

Figure 4: Single-Tone ADC FFT plot, F_{tone} = 1.2GHz

Further ADC testing included sending the 2000 tone comb from the DAC into the ADC (via a 2500MHz low-pass filter) and measuring the ADC NSD: -102.26 dBC/Hz. Additional tests included looking at channel-to-channel crosstalk on adjacent ADC and DAC channels and verifying the time-domain response of the DAC and ADC by playing out square and triangle wave signals from the DAC and recording with the ADC.

ACCELERATOR APPLICATIONS

Having verified the DAC and ADC perform within the desired specifications, we turn to some possible accelerator applications. Being targeted towards RF system applications, one such use would be for Low Level RF control. Direct down conversion is possible for some cases and low noise is advantageous. Another control application is intra- and coupled-bunch beam stabilization. For instrumentation, applications such as beam position and tune monitors, as well as bunch length, beam current and loss monitors. Beyond accelerators, particle detector systems are applicable. One such system is in development at SLAC.

WORK TO DATE

Following initial evaluation of the RFSoC, two projects have been targeted for this device. The first is the next generation of intra-bunch instability feedback control [10] development where transverse instability control requires high sampling rate and bandwidth. The second is a superconducting detector system: the SLAC Microresonator Radio Frequency (SMuRF) readout system [11]. In this system, frequency tracking is applied to many (2000+) detector channels which are frequency multiplexed across a 4GHz band. This detector system is implemented in the SLAC "Common Platform" (CP) [12] and plans exist to add RFSoC on another plug-in module to the CP portfolio of solutions.

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