LOW LEVEL RF TEST SYSTEM FOR THE COMPACT X-RAY LIGHT SOURCE AT ARIZONA STATE UNIVERSITY

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Abstract

A compact femtosecond X-Ray Light Source (CXLS) for time-resolved scientific and medical studies is being constructed at Arizona State University. The CXLS X-rays will be generated by the inverse Compton scattering (ICS) collision of 200 mJ, 1 ps, IR laser pulses with 300 fs electron bunches with energy up to 35 MeV. The electron beam is accelerated via a photoinjector and three standing-wave 20-cell linac sections driven by two klystrons delivering up to 6 MW 1 μs pulses at 9.3 GHz with a pulse repetition rate of 1 kHz. For initial testing of the CXLS klystrons a hybrid digital-analog low-level RF (LLRF) driver has been developed which allows for inter-pulse phase and amplitude corrections based on feedback from waveguide-couplers. The micro-controller based system can also be programmed to adjust continuously in advance of predictable drifts.

INTRODUCTION

The CXLS being constructed at Arizona State University is the first stage of a multi-year plan which will culminate with the world's first truly compact x-ray free electron laser (CXFEL). Generating x-rays via ICS the CXLS will be an incoherent source of ~10^8 photons per interaction of a relativistic electron bunch and an IR laser at 1 kHz. Here we report on development of the LLRF system, whose purpose is to both provide the initial drive signals which are amplified by two klystrons, before being fed into the RF-cavities to accelerate the electron beam, and to receive feedback from different points in the beamline to enable control to ensure the correct phase and power relationships are maintained between the different accelerating sections. The LLRF system presented here produces 700 ns pulses of 9.3 GHz RF that are amplified to 10 W by an X-band solid-state power amplifier (SSPA) (Microwave Amps, Ltd., AM73-06-001RB) and then up to 6 MW by the klystron (L3 Electron Devices, model L6145) powered by a modulator (ScandiNova, model K100). CXLS is powered by two modulator/klystron systems. Klystron 1 drives 2 RF structures. The first is a 4.5 cell photoinjector [1] accelerating the beam to 4 MeV. Electrons are generated at the photocathode using a UV laser which also triggers the ICS IR-laser. Klystron 1 also powers the first linear accelerator (Linac L1), a 0.35 m, 20 cell, standing wave RF-cavity [2] which is capable of accelerating the e-beam from 4 to 12 MeV. A second set of two linacs (L2 and L3) similar to L1 are powered by Klystron 2 resulting in a final beam energy of 35 MeV.

The LLRF system described here will be upgraded to a fully digital system based on the LCLS upgrade [3] in collaboration with SLAC.

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RF DRIVE CONTROL

The modulation scheme employed in the test-LLRF control system is Amplitude/Phase, as opposed to I/Q or Direct Digital Synthesis [4]. That is, our seed signal proceeds in series through electronic components which in turn modulate as required the amplitude and phase in response to feedback. The main controls element are microcontroller chips which are pre-programmed to run in a number of different control modes. This is in contrast to say systems controlled by Labview and commercial PXI systems [5] or ultra-fast FPGA based systems on more complex machines such as that for the International Linear Collider [6].

Seed Signals

The LLRF system provides the 9.3 GHz seed signal for the klystrons, which amplify these signals and fill the accelerating cavities. The initial 9.3 GHz driving master oscillator (MO) signal comes from a Wenzel Golden-Frequency Source which provides outputs at 76.65625 MHz, 2.325 GHz, 6.975 GHz, and 9.3 GHz.

The greatest noise beyond the carrier of the 9.3 GHz channel of the MO from 10 MHz to 13 GHz, are two sidebands at -81 dBc, their origin likely mixing with the 76.66 MHz frequency. The next highest noise peak -91 dBc, is at 6975 MHz, leaked from one of the other channels. The phase noise of the 9.3 GHz driving signal is shown in Fig. 1, the signal has single-sideband noise figures of, -116, -122, -126, and -136 dBc/Hz, at 1, 10, 100, and 1000 kHz.
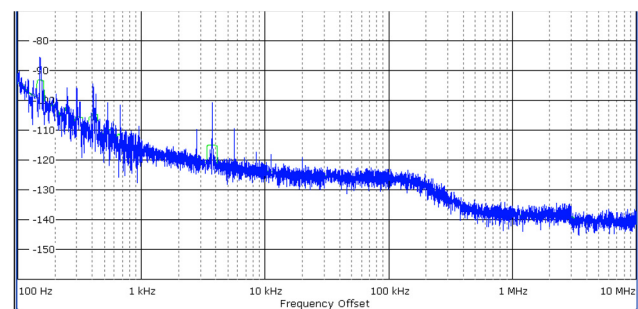

Figure 1: Single sideband phase noise plot of the 9.3 GHz seed signal.

Most of the noise seen in the plot of Fig. 1 is likely of mechanical/acoustic origin that has been mixed up to the carrier frequency. That the origin is most likely vibrational can be demonstrated simply. In Fig. 2 the spectrum around the carrier has been plotted with a 3.7 kHz tone from a laptop speaker either on or off. One way to overcome some of the microphonic disturbances is with piezoelectric devices in a feedback loop [7].
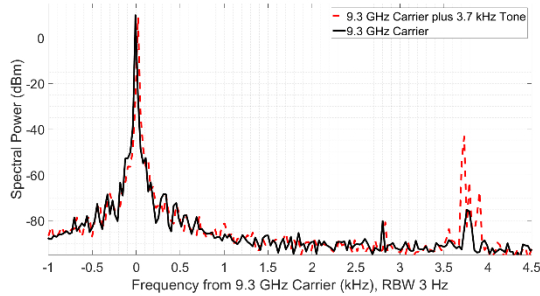
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Figure 2: Demonstrating acoustic noise mixed up to the carrier frequency.

The RF Seed Signal

A Stanford Research Systems (SRS) DG645 digital delay generator provides the trigger pulses which launch the 9.3 GHz seed signal for the klystrons. The timing of the DG645 and MO is disciplined via 10 MHz input from an SRS FS740 which contains a Rubidium oscillator. Long term timing is provided by the timing signals picked up from the GPS net-work. The locked highly stable output from the MO is continuous, hence an integrated RF switch (Analog De-vices, ADRF5020) is used to turn on and off the klystron seed signal. Switching outputs from off to on or vice versa takes ~20 ns, and another ~15 ns for full power throughput (or turn-off), from the start of the control signal. To reduce the risk of arcing the waveguides from the klystron are filled with SF6 at 45 psi. The waveguides have optical ports to which fibre-optic cables are attached. A reverse-biased photodiode circuit is linked to the enable input of the switch allowing complete shut-off of the RF-power to the klystron within ~40 ns.

The Need for Signal Modulation As there are two klystrons each powering different cavities the relative phase and amplitude of these sources must be tuned to ensure the electron bunches are accelerated as desired. Amplitude modulation is accomplished with an analog voltage controlled variable attenuator (VVA) (Analog Devices, HMC812ALC4) with a 30 dB attenuation range. In practice we do not need the full range and limit ourselves to a 10 dB range controlled by 0 to -5 V input. The analog phase shifter (Analog Devices, HMC247) has a range of ~300° and is controlled using a 0 to 10 V signal (see Fig. 3).

GPT simulations suggest the greatest timing sensitivity in the system is the laser-photoinjector timing where a ±0.5° phase shift results in a ±150 fs change in arrival time at the end of the beam line, and ±0.1% error in amplitude results in a ±30 fs delay. The sensitivity of the electron beam to errors in phase and amplitude drops by roughly an order of magnitude at each of the three successive RF accelerating structure beyond the photoinjector. The same ±0.5° phase error in either L1, L2, or L3, results in timing changes of ±3 fs, ±0.2 fs, and ±0.05 fs respectively. Similarly, amplitude error of ±0.1% at L1, L2, and L3 results in arrival time deviations of ±4 fs, ±0.4 fs, and 0.06 fs, respectively. From this we can understand that the major timing challenge is in synchronising the photo-cathode laser and the photoinjector phase, the other elements are orders of magnitude less sensitive.

Klystron Input Drive Chain

The output of the drive chain is ~0 dBm after insertion loss of the chain of around 10 dB (with the VVA set to minimum). The response of the klystron to seed input power is shown in Fig. 4. To reach 6 MW (97.78 dBm) requires an input of 42 dBm. The SSPA provides this gain to supply the klystron with an input of -15 dBm. Having the extra power is therefore helpful in addressing signal to noise considerations.
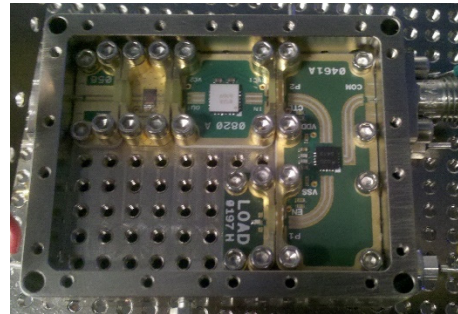

Figure 3: The first stage of the drive chain for the klystron during construction. The circuit blocks and housing were procured from X-Microwave.
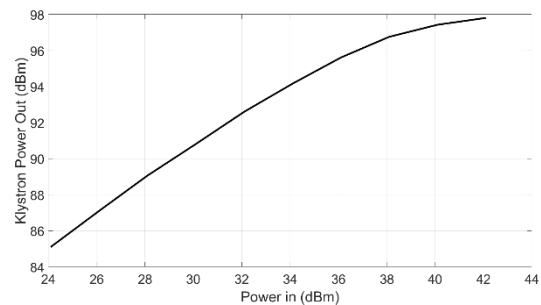

Figure 4: Measured power out from the klystron as a function of power in from the SSPA.

The setup is such that the change in power output close to the desired operating point of the klystron as a function of input is ~257.6 kW/dBm. The accuracy of the VVA is ±0.05 dBm which correlated to ±12.9 kW or ~±0.2% of the peak amplitude. Phase control of below 0.2° at 9.3 GHz has been verified with this setup. If necessary for ultra-fine slow tuning, a servo-adjusted mechanical attenuator between the SSPA and Klystron controlled by the LLRF control-board would allow changes of less than ±0.005 dB. Changing attenuation with the VVA causes phase changes, ~2°/dB, see Fig. 5. The phase shifter affects levels of attenuation at different rates depending upon the control voltage, see Fig. 6.
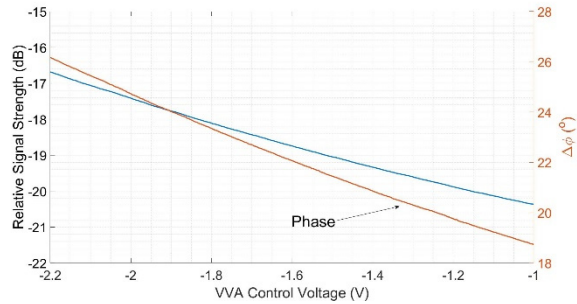
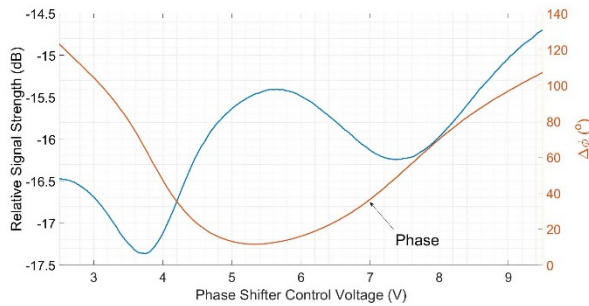Figure 5: Response of the VVA to control signals from the control circuit.

Figure 6: Response of the Phase-Shifter to control signals from the control circuit.

Sampling the High Power RF for Control

At the ILC and European XFEL many of the cavities run at 1.3 GHz, making direct sampling with ADCs a possibility [8]. However, to have a compact system CXLS was designed to operate in the X-band. Therefore down-conversion is required.

Waveguide couplers are positioned at various points downstream of the klystron with -60 dB coupling in order to measure the power and phase. These 9.3 GHz signals are to be mixed with the 6.975 GHz local oscillator (LO) to produce 2.325 GHz intermediate frequency (IF) that is fed into one of the inputs of a phase and amplitude comparison circuit based on the Analog Devices AD8302 chip. The IF signal reference for comparison is phase-locked 2.325 GHz output from the MO. For accurate measurement of phase difference the operating range of the AD8302 is limited to approximately -120° to -60° and +60° to 120° RF phase. RF cables roughly 8 m in length will introduce phase error due to thermal expansion and contraction, but with proper monitoring these slow changes should be simple to correct.

First Stage Control Circuit

A first iteration custom control circuit was designed, and assembled which allows for feedback and control of the drive chain. When triggered output from the AD8302 gain and phase comparison IC is amplified, sampled, and held, these voltages are transferred to analog-to-digital convertors (ADCs) which use serial peripheral interface (SPI) encoding to transfer the readings to a microcontroller (MCU) IC. The accelerator is designed to operate at 1 kHz repetition rate so the MCU has under a millisecond to read the ADCs and set the DACs controlling the VVA and Phase-

Shifter to different voltages if required. The slowest element is the VVA which requires ~250 μs settling time. The MCU is programmed to control the RF-circuit either from shot-to-shot under user control or in an autonomous mode maintaining a particular phase and amplitude balance. Changes are logged in an SD card on the board. There are sufficient IO pins to allow for control of other elements, such as fine-mechanical amplitude and phase control, even cavity tuners [9].

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