SOLID-STATE KLYSTRON MODULATOR FOR JLC

M. Akemoto, Y. H. Chin, Y. Sakamoto, KEK, Tsukuba, Japan

Abstract

The klystron modulator for the Japan Linear Collider (JLC) is required to produce a 500 kV, 530 A, 1.5 μs flat-top pulse, and to drive a pair of 75 MW PPM-klystrons. To improve the reliability and energy efficiency, we are developing a solid-state modulator with a 1:5 primary split pulse transformer. This modulator consists of two parallel modulator units, each driving the primary winding of the transformer. Each modulator unit uses multiple pulse modulators stacked in series, and generates 50 kV, 2650 A pulses. This allows fast over-current protection and easy-to-control flat-top tuning of the output waveform. In our present study, a ten-stage test modulator has been built and has been successfully operated at 20 kV and switched up to 2860 A.

1 INTRODUCTION

The energy efficiency, reliability and costs of the klystron modulators are extremely important. Their improvements are a major challenge in a large-scale linear collider, such as the JLC[1]. In order to improve the reliability of a line-type modulator, we have already developed a 45 kV solid-state switch using SI-thyristors to replace the thyratron tubes[2]. Now, we are developing a new hybrid modulator with a number of individual pulse modulator stages in series and a pulse transformer. To study a modulator of this type, a ten-stage test modulator has been built and tested. In this paper, we describe this JLC modulator design, and the experimental results of the test modulator.

2 JLC MODULATOR

2.1 Modulator Design

The klystron modulator for the JLC is required to produce a 500 kV, 530 A, 1.5 μs flat-top pulse to drive a pair of 75 MW PPM-klystrons[3]. Table 1 lists the specifications of the JLC klystron modulator. The JLC hybrid modulator uses multiple individual solid-state modulators (cell-modulators) which are stacked in a voltage-adder configuration and a 1:5 primary split pulse transformer. Figure 1 shows the basic circuit diagram of the JLC klystron modulator. Each cell-modulator is a direct switching modulator which is capable of generating a 2 kV pulse at 2650 A. Some cell-modulators are used as a waveform control modulator to obtain an output waveform with a wide flat-top. The modulator unit, which consists of 26 cell-modulators stacked in series and which generates a 50 kV pulse at 2650 A, drives one of the primary circuits of the pulse transformer. The other unit also drives the other primary circuit. The pulse transformer provides the klystrons with a 500 kV pulse. The inverter charging system provides DC power to each cell-modulator.

Table 1: JLC Klystron Modulator Specifications.

Parameter	**Value**
Peak Klystron Voltage	500 kV
Total Peak Current	530 A
Pulse width(flat-top)	1.5 μs
Pulse Top Flatness	2%
Energy Efficiency(Goal)	70%
Repetition rate	150 Hz

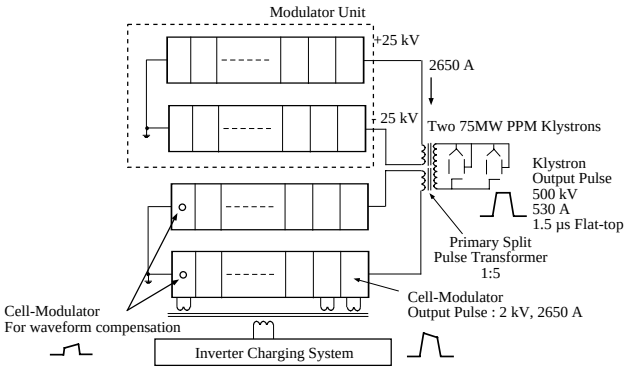

Figure 1: Basic circuit diagram of the JLC klystron modulator.

2.2 Cell-Modulator

A unit of the cell-modulator consists of an energy storage capacitor and a solid-state switch, which turns on and off the circuit. It also includes a bypass diode which protects the solid-state switch and provides isolation with respect to the other stages. The cell-modulator works as follows. The capacitor is initially charged through a charging transformer. When the switch is turned off, as shown in Fig. 2(a), the cell-modulator is completely separated from the output circuit, and the output current flows through the bypass diode. When the switch is turned on, as shown in Fig. 2(b), the current in the diode is commutated. The energy storage capacitor is now connected in series with the output circuit, and the charging voltage of the energy storage capacitor is added in the output circuit. Both the pulse width and timing of

the output pulse of the cell-modulator are determined by controlling the gate trigger of the switch.

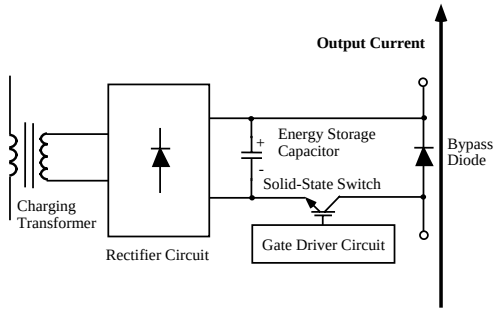

Figure 2(a): Cell-modulator when the switch is turned off.

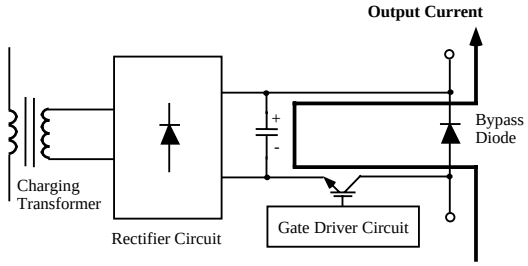

Figure 2(a): Cell-modulator when the switch is turned on.

3 10-STAGE TEST MODULATOR

3.1 Circuit

Figure 3 shows a circuit diagram of a 10-stage model modulator. It consists of 10 cell-modulators stacked in series, a charging system to provide DC power to each cell modulator, and a resistor load. The design parameters of the model modulator are given in Table 2. A photograph of the stack assembly with a resistor load is shown in Fig. 4.

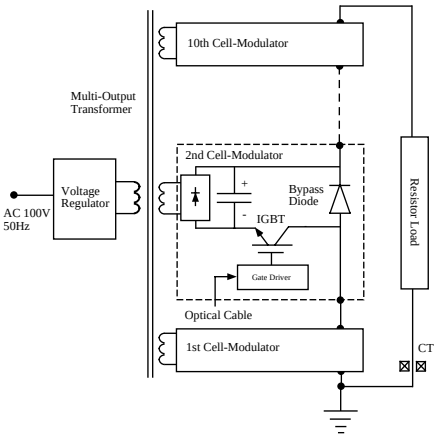

Figure 3: Simplified schematic of a 10-stage test modulator circuit.

Table 2: Design parameters of a 10-stage test modulator.

Parameter	**Value**
Output Voltage	20 kV
Output Current	2.7 kA
Pulse Width	3 μs
Number of Cell-Modulator	10 stage
Repetition Rate	5 Hz

A photograph of a cell-modulator is shown in Fig. 5. An Insulated Gate Bipolar Transisitor (IGBT), MITSUBISHI CM1200HB-66H, was used as a solid-state switch. The CM1200HB-66H is rated at 3.3 kV peak voltage and 1200 A average current. The gate drive circuit for each IGBT receives its trigger pulses from a trigger control circuit through optical cables. The capacitance of the energy capacitor was determined to be 17.3 μF in order to keep its voltage drop within 10%. The capacitor of each cell-modulator is charged through a multi-output transformer. The output voltage of the modulator is regulated by adjusting the charging voltage of each cell-modulator. The output current of the modulator was measured with a Pearson's current transformer.

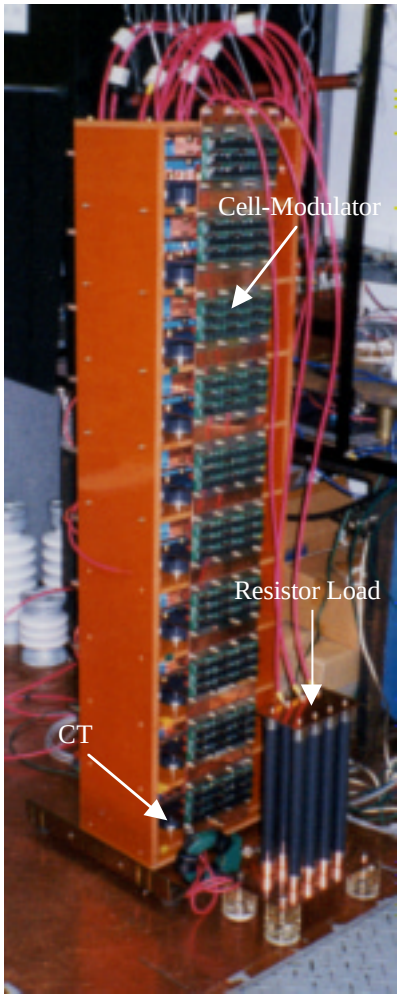

Figure 4: 10-stage test modulator with a resistor load.

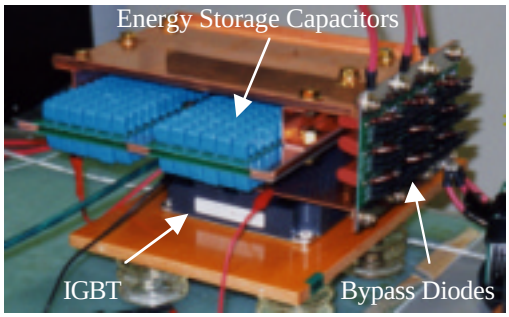

Figure 5: A cell-modulator.

3.2 Output Waveform

Figure 6 shows an example of the waveform of the output current through a 5.2 Ω resistor load. In this test, 10 cell-modulators were used, and each modulator was operated at a voltage of 1.7 kV. A pulse with a peak voltage of 17 kV, a peak current of 2890 A, a rise time(10-90%) of 770 ns and a fall time of 580 ns was successfully generated. The output pulse has a droop of approximately 10%, which is consistent with the expected droop in the energy storage capacitor.

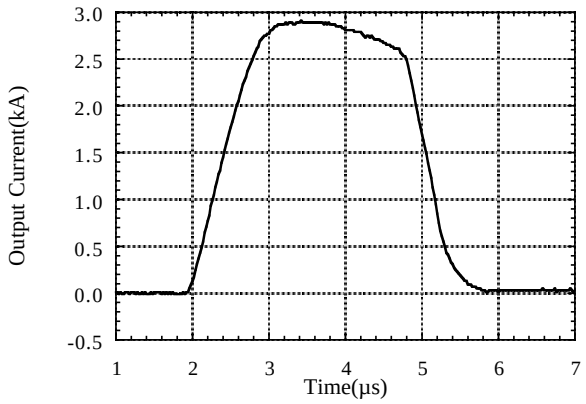

Figure 6: Output current waveform.

3.3 Waveform Control[4]

We have tried to control the output waveform with appropriate triggering of cell-modulators. In this test, a set of 10 cell-modulators (stages) was operated at a voltage of 1 kV with a 4.1 Ω resistor load. The first and second stages were used as a waveform compensation modulator. In order to obtain the maximum flat-top width, the trigger timings for the first and second stages were adjusted. Figure 7 shows the trigger timing for each stage. Figure 8 shows the output current waveform at the resistor load, with and without waveform compensation. The output waveform without compensation was drooped with no flat-top, but the compensated waveform became rectangular with a wide flat-top. From this result, we found that individual trigger control for the cell-modulator enables us to produce an excellent waveform with a wide flat-top, which improves the power efficiency.

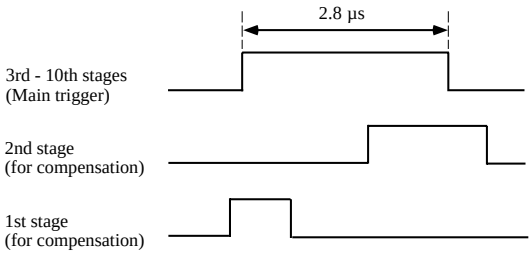

Figure 7: Trigger timing chart.

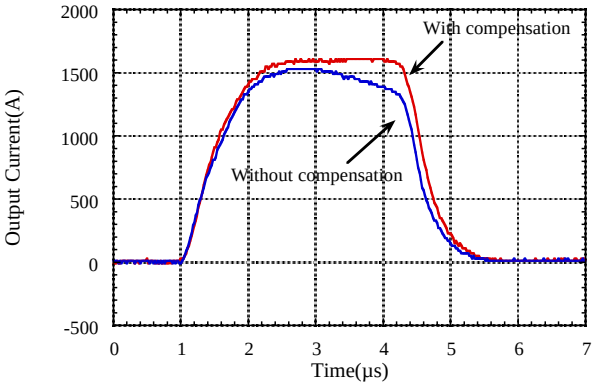

Figure 8: Output current waveform with and without compensation.

4 FUTURE R&D

Testing of the fast over-current protection for the IGBT will soon be performed using the 10-stage test modulator. High-power testing with a primary split pulse transformer will also be carried out to study the performance of the modulator. We also plan to build a full prototype modulator capable of driving two 75 MW PPM-klystrons at a 100 Hz repetition rate by 2002.

5 REFERENCES

[1] JLC Design Study Group, "JLC Design Study," KEK Report 97-1, 1997.

[2] M. Akemoto et al., "High-Power Switch with SI-thyristors for klystron Pulse Modulators," Conference Record of the 2000 Twenty-Forth International Power Modulator Symposium, Norfolk, Virginia, USA(2000) 205.

[3] Y. H. Chin et al., "Status of the X-band RF Power Source Development for JLC," Proc. of EPAC 2000, Vienna, Austria(2000) 456.

[4] M. Akemoto et al,, "Improvement of Waveform Efficiency Using a Compensation Circuit," Proc. of LINAC 2000, Monterey, California, USA(2000)769.