NEW APS STORAGE RING BPM TIMING SYSTEM DESIGN *

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Abstract

A new beam position monitor (BPM) timing system has been designed for the Advanced Photon Source (APS) storage-ring. The old system used beam-derived triggers. The timing system provided a gate to determine which stored bunch would be processed. While this system served the APS well, it was determined that an rf-derived trigger system would reduce unwanted effects such as measured position intensity dependence. The new BPM timing system provides independently settable rf-derived timing triggers for each BPM. The system uses an existing module design to provide rf-derived triggers for each stored bunch in conjunction with a new module design that selects rf-derived triggers and provides independent delays for each BPM within a sector. The system provides the flexibility to trigger on single or multiple bunches per turn and supports arbitrary trigger patterns of up to 400 turns in length. The design and performance of this new system are discussed.

1 INTRODUCTION

The Advanced Photon Source has 360 rf monopulse receiver beam position monitors (BPM). Each BPM has an associated signal conditioning and digitizing unit (SCDU). SCDUs, as originally designed, triggered on the beam signal. Timing provided an "arm" signal, which selected the stored bunch each SCDU would use as a trigger [1]. The SCDU used a threshold comparator circuit for the beam-derived trigger and thus suffered from an intensity-dependent trigger walk. This trigger walk manifested itself as position dependence with beam intensity.

The desire to reduce the BPM systems' intensity dependence prompted a redesign of the storage-ring BPM timing system. This effort changed the function of BPM timing from serving as a gate for bunch selection to providing a storage-ring rf-derived timing trigger for each of the 360 BPMs. Each SCDU required a relatively simple modification to transform the timing "arm" input into a trigger input. The remainder of this paper will focus on BPM timing trigger generation.

2 OVERVIEW

Figure 1 shows a simplified picture of the BPM timing hardware installed at each BPM input-output controller (IOC) VME crate. Four timing signals are distributed from the central timing system: the storage-ring revolution clock, a 44-MHz clock derived from the storage-ring low-level rf, a trigger inhibit, and an initialize.

A key component of the timing system is the bunch clock generator (BCG) module, which has been previously described [2]. The BCG was originally designed to provide timing triggers to beamlines. It serves a similar purpose in this application. The BCG is programmed to provide a trigger pulse for each stored bunch. The pattern of bunch clock triggers repeats each storage-ring revolution. New modules were designed to provide a programmable means of selecting which bunch trigger to pass on as a trigger pulse to the SCDUs. The remainder of this paper will focus on the design and integration of these new BPM trigger modules.

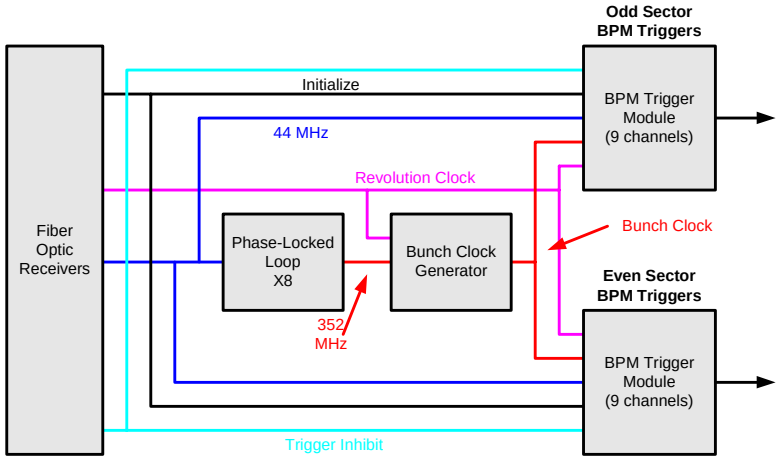

Figure 1: BPM timing block diagram.

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3 RF REFERENCE DISTRIBUTION

Each BCG requires two input signals: the storage-ring revolution clock and the storage-ring rf frequency (351.9 MHz). Twenty-three BCGs are required – one for each of the 23 BPM IOCs. A key issue is how to distribute the 351.9-MHz rf to each of the remote locations. Since "dark" multi-mode fiber optic cable was available at each IOC, a scheme reported in an earlier paper [3] that allowed the use of such fiber was selected. This scheme digitally divides the 351.9-MHz storage-ring low-level rf by eight to generate a phase-related and frequency-locked 44-MHz signal. The 44 MHz is easily distributed via multi-mode fiber with low-cost fiber optic components. Each IOC contains a phase-locked loop that multiplies the 44 MHz by eight to reconstruct the 351.9-MHz storage-ring rf signal required by the BCG modules.

4 BPM TRIGGER MODULE

Figure 2 shows a simplified diagram of the BPM trigger module. This module replaced the VXI BPM timing module described in reference [1]. It provides the nine output triggers for a single sector of SCDUs. Forty of these modules are required to trigger the 360 SCDUs distributed in 40 VXI crates.

The circuit is based on a programmable arbitrary bit pattern generator (ABPG). The ABPG is programmed to select desired bunch triggers from the BCG. Each selected bunch trigger drives nine programmable delays that provide the nine BPM timing triggers required for a sector of BPMs.

The ABPG in the BPM timing module runs at one-eighth the clock rate of the BCG. This translates to a resolution of eight rf buckets: in general, the BPM timing module cannot resolve bunch triggers that are spaced less than eight rf buckets apart. This is not a problem because the SCDUs are not capable of resolving bunches that closely spaced.

The ABPG has sufficient memory to store a pattern equivalent to 404 storage-ring turns. The pattern length in turns is programmable. The initialize signal, which is distributed to all BPM timing modules, resets the pattern length counter. This provides the means to synchronize all 40 BPM timing modules to begin multi-turn patterns on the same turn.

The programmable delays are based on the AD9500 digitally programmable delay generator [4], which provides an 8-bit settable delay. A resistor and capacitor set the delay range. For this application, the range is set to 280 ns, which corresponds to about 1.1 ns per bit. The 280-ns range was selected to cover the worst-case delay between BPM signals over a single sector. A fixed 100-ns delay (not shown in Fig. 2) may be switched in, which delays all nine outputs by an additional 100 ns. This feature is provided to accommodate sector-to-sector delays for the 17 IOCs that handle double sectors of BPMs.

It is critical that the ABPG output be timed to the BCG output to provide the proper gating function. Programmable fine and coarse delays are provided. The coarse delay shifts the ABPG output in 44-MHz ticks, while the fine delay shifts the ABPG output in 100-ps steps. A test output (also not shown) is used to determine the proper coarse/fine delays to time the ABPG output to encompass the BCG output.

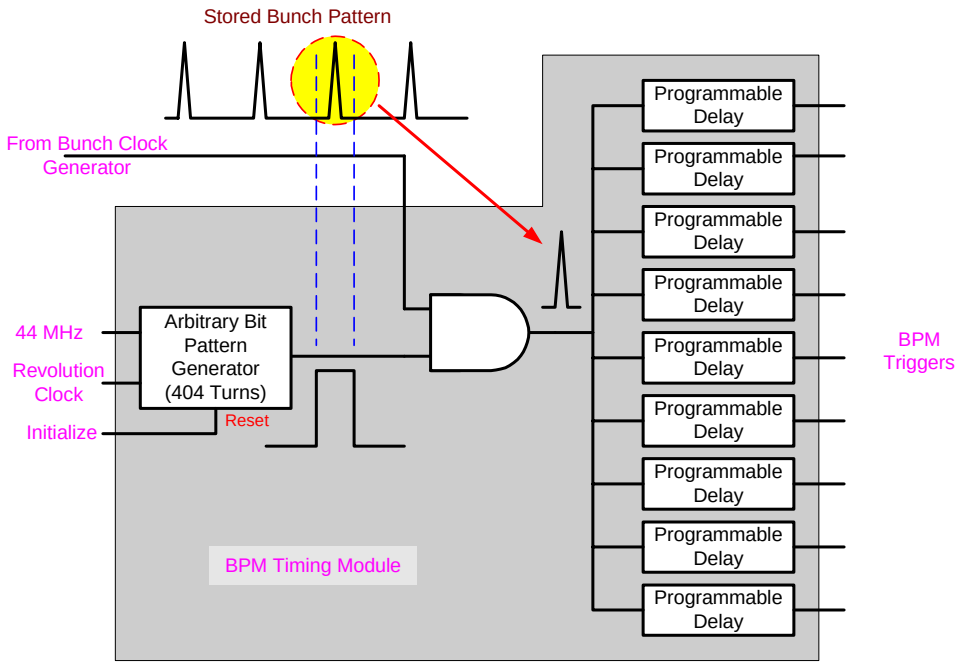

Figure: BPM timing module block diagram.

The ABPG is implemented with a programmable logic device and CMOS static RAM. The circuitry for the BCG path (including the AND gate shown in Fig. 2) is implemented with emitter coupled logic.

5 SOFTWARE

Both the BCG and the two BPM timing modules have coarse/fine delays for their pattern generators. An EPICS database was designed that permits these six values to be manipulated in a coordinated manner. Three EPICS process variables are used. The first two define the offset in nanoseconds between the BCG output and the two BPM timing module ABPG outputs. These process variables are adjusted with the aid of an oscilloscope to delay each of the ABPG outputs with respect to the BCG so that each ABPG properly acts as a gate for the BCG output.

The third process variable sets the time of the combined outputs relative to the storage-ring revolution clock. This process variable is adjusted to time shift the nine triggers of each BPM timing module relative to the beam. The EPICS database combines the offset process variables with the time relative to the revolution clock to compute fine/coarse delays for all three modules.

In addition, an EPICS sequence program is provided that loads either a default pattern into each module or the actual stored bunch pattern obtained from the timing system.

New and yet untested is a bunch-cogging feature. Normally the BPM timing is set to trigger on a six-bunch BPM timing group. The cogging feature implemented in the sequence program sets the pattern in the BPM timing modules to rotate through all bunches on successive storage-ring turns. Thus, the reported beam position will be an average of all stored bunches. This should be of particular value for further reducing intensity dependence while the storage-ring is operated in “top up” mode.

6 PERFORMANCE

The most significant performance figure is the time jitter in the output triggers relative to the storage-ring low-level rf. There are two main contributors to jitter in the outputs: the phase-locked loop and the AD9500 digital delays. The overall jitter of an output trigger is about 0.8 to 1.0 ns peak-to-peak with an RMS of less than 150 ps. A large fraction of the jitter is due to the AD9500 devices. The timing jitter translates into noise on the position measurement with a magnitude determined by the “flatness” at the trigger time of the BPM signal presented to the SCDU. Timing scan measurements show that the peak-to-peak jitter has no significant impact on position measurement. Other programmable delay devices that exhibit considerably less jitter were evaluated, but discarded because they are significantly more costly.

Preliminary measurements show that measured bunch-to-bunch crosstalk [5] and position dependence on intensity are significantly reduced with the new timing scheme.

7 CONCLUSION

The new BPM timing system was initially installed and tested in sectors 25 and 26 in October 2000. Installation in all sectors was completed during the April 2001 shutdown and is now providing timing for all 360 storage-ring mono-pulse BPMs.

8 REFERENCES

[1] F. Lenkszus, E. Kahana, A.J. Votaw, G. Decker, Y. Chung, D. Ciarlette, R. Laird, “Beam Position Monitor Data Acquisition for the Advanced Photon Source,” PAC93, Washington, D.C. (May 17-20, 1993), **3**, 1814-1816.

[2] F. Lenkszus, R. Laird, “A Bunch Clock for the Advanced Photon Source,” PAC97, Vancouver, BC, (May 12 - 16 1997), **2**, 2490-2492.

[3] F. Lenkszus, “State-of-the-Art Developments in Accelerator Controls at the APS,” PAC99, New York, N.Y. (Mar. 29 – Apr. 2, 1999), V. **1**, 333-337.

[4] Analog Devices, Norwood, MA.

[5] R. Lill, G. Decker, O Singh, “Advanced Photon Source RF Beam Position Monitor System Upgrade Design and Commissioning,” DIPAC, Grenoble, France, May 2001.