THE SNS LINAC RF CONTROL SYSTEM*

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Abstract

Development of the Spallation Neutron Source (SNS) continues, with operations beginning in 2004. The SNS is a 1 GeV machine consisting of a combination normal-conducting and super-conducting linac as well as a ring and target area. The RF control system (RFCS) for the linac has been under development for two years, with the first versions of the individual modules under construction and system integration begun. This paper will discuss this stage of the design and its implementation. In addition, it will report on the module variations required to use similar hardware for both the normal conducting (NC) and superconducting (SRF) portions of the linac.

1 TOP LEVEL

The RF Control System (RFCS) is required to provide ±0.5% amplitude and ±0.5° phase stability of the cavity fields throughout the linac. Feedback and feedforward control techniques are used to achieve these control specifications. Other functions of the RFCS include the detection and shutdown of the RF drive to the klystrons should a fault occur in the high power RF transport system and cavity resonance monitoring and control. A subsystem of the RFCS provides for distribution of the phase-stable RF reference signal at both 402.5 MHz and 805 MHz. The following figure depicts these functions in block diagram form.

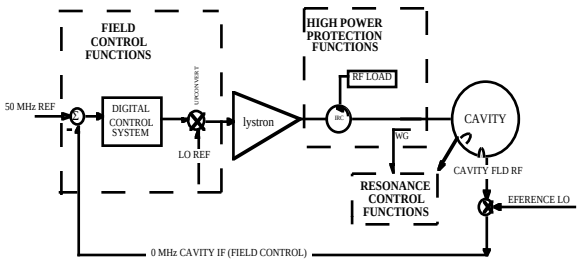

Figure 1: RF Control System block diagram.

2 VXIBUS MODULES

This paper focuses on the hardware design (which is supported by extensive computer modeling) and its current status [1]. The RFCS primarily consists of three LANL-designed VXIbus modules which are further described below. The first revisions of these printed circuit boards are under development

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2.1 Clock Distribution Module

The Clock Distribution Module (CDM) synchronizes the various system clocks with the 2.5 MHz master oscillator (also part of the RFCS) which is distributed along the klystron gallery and tapped off at each RFCS. The CDM accepts and distributes the timing signals received from the Machine Timing System (*e.g.:* RF Gate, synchronous sample) to the other RFCS modules. The Timing System is responsible for synchronizing the RF with all other machine systems such as beam, chopper, target, *etc.* The CDM has two phase-locked loops locked to the master oscillator's 2.5 MHz reference routed in RFI-protected channels on the printed circuit board (PCB). The PLL outputs are used for clock synchronization within the RFCS, for demodulating the cavity IF, and for upconversion of the controlled cavity IF. This module has two build versions: one for 402.5 MHz and one for 805 MHz; otherwise the layout is the same for both the NC and SRF cavities. The PCB is at the manufacturer now. An ECAD layout is shown below.

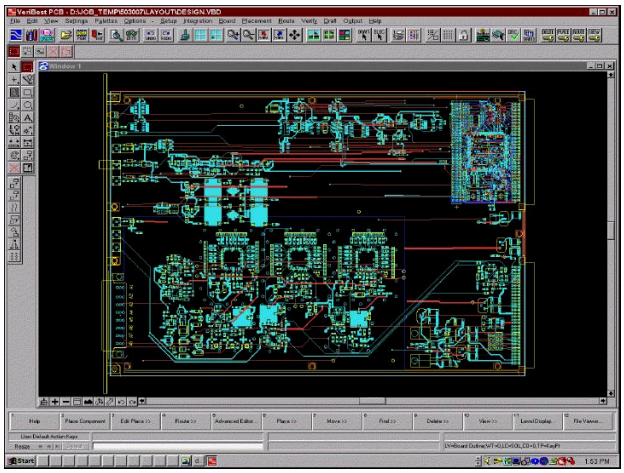

Figure 2: Clock Distribution Module PCB

2.2 High Power Protect Module (HPM)

The High Power Protect Module (HPM) provides fault protection for the RF transport system by disabling the RF drive upon a high reflected power trip, cavity arcs, *etc*. This board relies on a RF front end and a digital logic interface. Altera Programmable Logic Devices (PLDs) in the logic portion allow for user-defined settings. This provides us with the flexibility to change the logic without changing the hardware, should the original High Power Protect requirements be modified as we begin commissioning the accelerator. The HPM will monitor up to seven RF channels (set by the RFQ requirements). All of the HPMs will be built the same with the detectors

calibrated at 402.5 MHz or 805 MHz, depending on their application in the system. The fault threshold and duration settings are all settable *via* the EPICS software thereby allowing the same board to be used for the different cavity types. Both the CDM and HPM are single-wide VXIbus modules.

2.3 Field / Resonance Control Module (FRCM)

The third LANL module, the Field and Resonance Control Module (FRCM) is a double-wide VXIbus module consisting of a motherboard and three daughter boards. The motherboard provides power conditioning and communication between the daughter boards and the global computer control system (EPICS) *via* the VXIbus backplane. It also performs the fast control algorithms in PLDs as well as a number of internal diagnostics. In order to perform all of this, the motherboard is a fully loaded, 16-layer digital printed circuit board with 5 Altera PLDs. The PCB is in layout now, with a preliminary ECAD layout shown below.

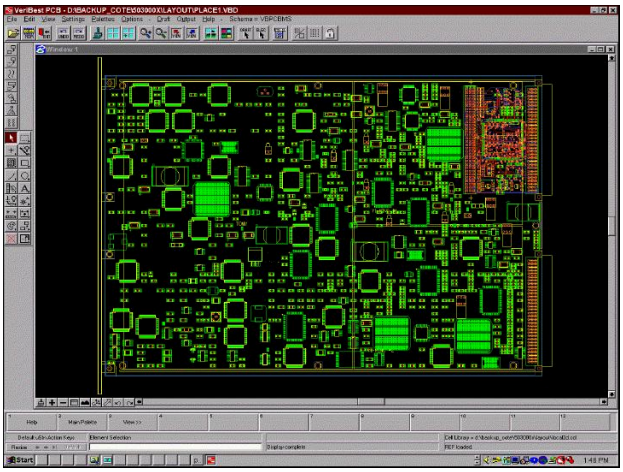

Figure 3: Motherboard PCB layout

There are two types of daughter boards. The RF daughter board processes the accelerator RF and IF signals (e.g., Field Sample, Klystron Forward Signal) and translates them into their baseband in-phase and quadrature (I/Q) components. Figure 4 shows the ECAD layout of this daughter board. This board is all FR4 substrate and relies on coplaner stripline for the RF signals.

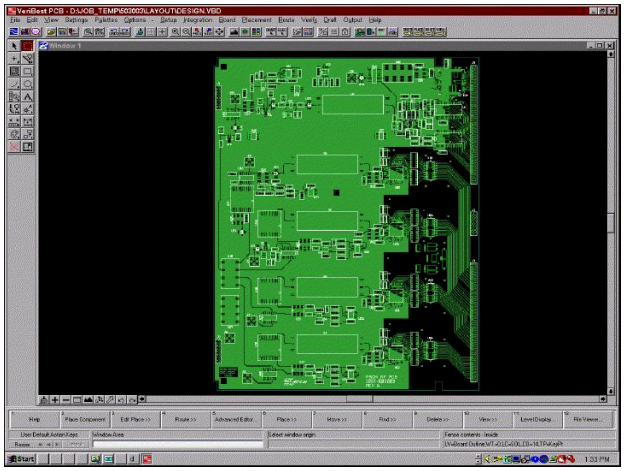

Figure 4: RF daughter card.

The other daughter boards are both DSP-based. One is used for determining the resonance condition of the cavity and sending an error correction signal to the cavity resonance control system (water cooling for normal conducting and mechanical tuner for superconducting cavity), and the other does all of the supervisory computations, as well as feedforward algorithms, etc. The plan is to build the first sets of each PCB in-house before going to a contract house for manufacture and assembly. However, because of the ball-grid array (BGA) architecture of our digital signal processor (TI's TMS320C6203GLS), the DSP daughter boards are both being manufactured and assembled by an outside vendor. Although we encountered the expected 'interaction learning curve' with the vendor, the process has gone fairly smoothly and we have confidence in going back to them for manufacture and assembly of the production run. We will provide the vendor with parts kits, while they will be responsible for both the PCB fabrication and assembly. The first assembled board is expected at LANL the week of June 25, 2001.

In relation to the motherboard, the RF daughter board is mounted on the left side. The two DSP daughter boards mount on the right side of the motherboard, one in the upper right quadrant, and one in the lower right quadrant. (This is faintly delineated in figure 3).

3 NC *VS.* SRF

As noted, the SNS RFCS is based on a digital architecture which will allow us to use the same hardware design for both normal conducting (NC) and superconducting (SRF) cavities. We simply download new firmware as needed for each application. For example, different RF-on algorithms will be used for initially injecting RF into each cavity type to take full advantage of the control margin provided by the klystrons [2] and to meet the cavity requirements. The fill-time of the cavities varies by an order of magnitude, *e.g.:* 20 μs for the DTL versus 200-250 μs for the SRF cavities. With one of the DSP daughter boards, we can implement

the correct set point profile for each cavity. The same idea applies for Lorentz force detuning. Lorentz force detuning, which occurs only in the superconducting cavities. In order to minimize the effects of the Lorentz Force detuning, we will simply send a signal to the cavity tuner to pre-detune each SRF cavity. We can use the same hardware module and not send this pre-detune signal for the NC cavities. The digital foundation of our designs allows us to complete the hardware designs now, and modify the firmware as the specifications evolve.

Because we have a single 'RF-off' input from the Machine Protect System, we can provide RF shutdown based on any type of system-level fault (*e.g.*: bad vacuum - RFQ; poor Helium pressure – SRF; mechanical tuner has entered a 'hunting' mode - SRF). We rely on the Machine Protect System to determine if a RF-off condition is required and to trip the hardware as appropriate. In this manner, we have the agility to accommodate a variety of types and number of interlocks. System designers have modified the requirements for RF trip conditions as the accelerator design has progressed, and in all likelihood, this will continue. Experience has shown that as we commission the accelerator, unforeseen operational requirements will become necessities. With the agile hardware designs that we have now, we believe that we can adapt to the new requirements by simply downloading new code into the existing modules.

4 SUMMARY

A Final Design Review of the RF Control Systems for the superconducting part of the accelerator will be held in August, 2001. In the meantime, progress on the hardware continues. Two of the prototype printed circuit boards have been built. The RF daughter board is being assembled this week. A fully assembled DSP daughter board should be received from the contract manufacturer next week. The CDM has recently gone out for fabrication and the HPM should go out for fabrication in one to two weeks. Only the FRCM motherboard remains in ECAD, at the beginning of the board's layout cycle. The next steps are to test the modules as single entities and then integrate them as a prototype system. We expect to be doing that this fall. It is anticipated that a "first article" version of each module will then go back to ECAD for re-work and then assembly and test. Early next year we should be fielding our first official RF Control System for the SNS RFQ (which is being built at Lawrence Berkeley Laboratory).

5 REFERENCES

[1] S.I. Kwon, "Uncertain System Modeling Of SNS RF Control System," PAC'01, Chicago, June 2001.

[2] M.T. Lynch "Excess RF Power Required for RF Control of the Spallation Neutron Source (SNS) Linac, a Pulsed High-Intensity Superconducting Proton Accelerator," PAC'01, Chicago, June 2001.