A TIMING-REFERENCE GENERATOR FOR POWER-GRID-SYNCHRONIZED NEUTRON-SPALLATION FACILITIES

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Abstract

Accelerator-based neutron-spallation facilities often derive their internal timing reference from the AC-power grid. Because the grid-frequency fluctuates, there is an inherent conflict between the performance of accelerator systems and neutron choppers. An optimal solution to this problem is to provide a phase-locked timing-reference signal with enough coupling to the grid to meet accelerator demands and enough de-coupling to meet chopper requirements. This paper describes the design and operation of a LANSCE-12-developed DSP-based timing-reference generator suitable for grid-synchronized facilities. It outputs a phase-locked, nominal 120-Hz pulse train. The amount of grid coupling or output pulse-to-pulse filtering can be set by the user to any of 10 discrete levels. The paper also includes a description of the real-time dual-loop control algorithm running in the DSP, how different loop parameters are used at each control point and performance results.

1 INTRODUCTION

Many accelerators around the world derive their internal timing and trigger references from their local AC-power grid. The accelerators at Los Alamos and Argonne are examples of this type. The Spallation Neutron Source (SNS) is also being designed to be linked to the AC-power grid for timing and synchronization.

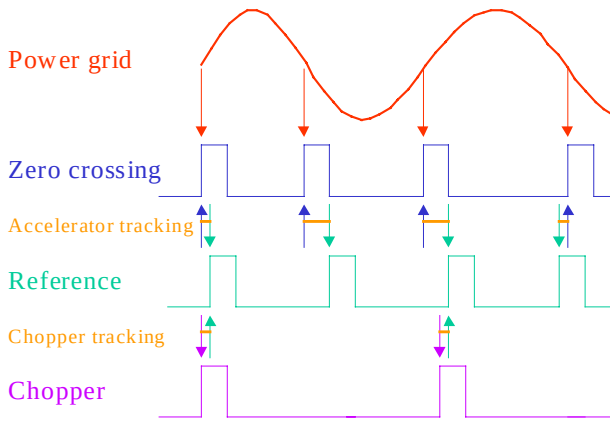

Figure 1. Timing waveforms and relationships.

The power grid in the U.S. is not a constant 60 Hz and suffers from small frequency and phase fluctuations which show up as cycle jitter and gained or lost cycles over time. The timing relationship between the grid, zero crossings, reference and chopper signals is shown in figure 1.

Accelerator-tracking and chopper-tracking sigmas as well as system-wide and chopper timing requirements have been described in references [1,2,3]. As a brief review, the accelerator tracking sigma, measured as one standard deviation of the time interval between the zero-crossing and reference signals, is a measure of how closely the reference tracks the grid.

The chopper-tracking sigma is measured as one standard deviation of the time interval between the reference and a chopper's output synchronization pulse. Typically, 1000 points are used to compute the standard deviations.

Most accelerator sub-systems, such as instrumentation, control, and RF power, are not adversely affected by timing jitter and wandering grid phase. However, other systems, such as neutron choppers or other low-bandwidth slow-response devices, are unable to track the fast variations in the line phase and would prefer a stable clock or be de-coupled from the grid.

Normally, choppers must be properly phased to the timing reference signal they use so that they can block or chop the neutrons that are supplied to them at a certain and specified time in each cycle.

An optimal solution to this problem is to provide a phase-locked timing-reference signal with enough coupling to the grid to meet accelerator demands and enough de-coupling to meet chopper requirements. This paper describes a phase-locked timing-reference generator developed at LANSCE-12 that allows the user to set the amount of reference-signal coupling to the grid thereby allowing for optimal operating performance of both the accelerator and choppers.

2 HARDWARE

The block diagram of the Timing-Reference Generator is shown in figure 2. In general terms, the generator consists of input signal conditioning hardware (an analog card), a digital card, and an Innovative Integration Inc. SBC32 TMS320C32-based DSP board.

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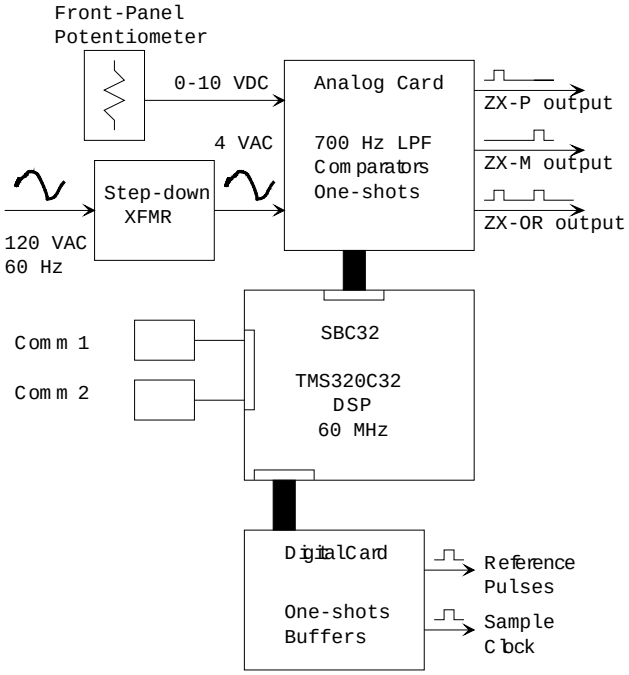

Figure 2. Block diagram of the timing-reference generator hardware.

The SBC32 has four ±10V 16-bit ADCs and four ±10V 16-bit DACs. The 32-bit floating-point DSP runs at 60 MHz and has two 32-bit internal counter/timer registers that are clocked at 15 MHz. One is used to set the periodic 3-kHz sample rate, and the other used to generate the phase-locked 120-Hz reference pulses.

A step-down transformer provides a 4-VAC signal to the analog card where it is filtered by a 700-Hz single-pole RC low-pass filter and then supplied to the DSP card. This filtered signal is also applied to a couple of comparators and positive and negative zero crossing pulses are generated and provided as user outputs.

A front-panel precision potentiometer is used as a simple means to control the set point. Its output is 0 to 10 VDC which the DSP reads, discretizes and interprets as a control level. A ribbon cable connects these analog-type signals to the DSP board.

The digital card connects to the DSP card by a ribbon cable and contains simple one-shots and digital buffer/line-driver TTL circuitry. Two outputs are provided for the user. One is a sample clock pulse train which can be viewed to confirm the 3-kHz system sample rate. The other output is the phase-locked smoothed timing-reference pulse train.

Two RS-232 communications ports are available to the user. Port 1 is used to program the SBC32's flash PROM. Port 2 was programmed to output ASCII status information such as control level, measured frequency, output frequency, and time difference between the reference and output signals. This has been successfully connected to a National Instruments ENET-232/4 serial to Ethernet device and served over the local network.

3 THEORY OF OPERATION

The Timing-Reference Generator is based on and uses a programmable, real-time, dual-loop, feedback control system implemented within the DSP. The inner loop controls the velocity or frequency, and the outer loop controls phase.

The algorithm first detects the frequency of the grid, and multiplies it by two. It feeds this value forward to the velocity-loop triple-summing block. The zero-order hold after the triple summing block models the 120-Hz internal-loop discrete-sampling rate. A PI controller block amplifies the velocity error signal and feeds it to a discrete-time-domain IIR single-pole low-pass filter. This filter is the primary design element of the timing-reference generator. Its design bandwidth ranges from 0.05 to 5 Hz and sets the fundamental response of the entire model and the overall ability to track the grid. The value of this filter also determines the amount of jitter removal from the output pulse train. A software limiter on the output of the filter ensures that the output frequency is within 120 ± 1 Hz. The output frequency is then integrated and multiplied by 2π to obtain radian phase for the outer control loop.

The reference phase is derived from the grid zero

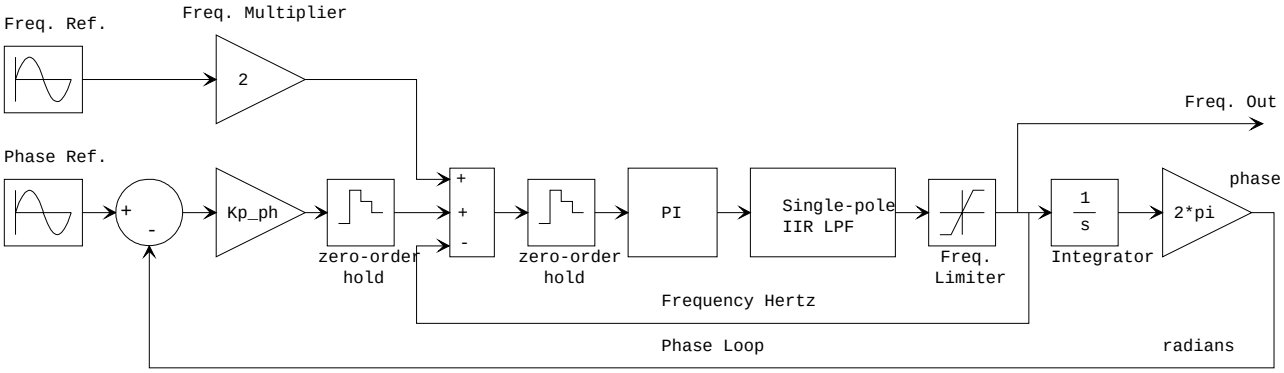

Figure 3. MATLAB/Simulink model used to design and program the DSP.

crossings and fed to the outer loop summing block where it is compared with the feedback phase value. The phase error is then forwarded to a gain block, Kp_ph, where it is amplified, sampled with a zero-order hold running at 120 Hz, and then fed to the triple-summing block.

The system is tuned by first tuning the inner velocity loop and then the outer phase loop. The velocity loop is tuned by selecting the desired filter cut-off frequency, calculating its coefficients, setting the outer phase-loop gain to zero, and adjusting the PI coefficients for a stable frequency response.

When operating, at each control level, the DSP calculates the necessary coefficients for the velocity-loop PI block, the digital filter, and the phase loop Kp_ph block.

4 PERFORMANCE

The user can set the Timing-Reference Generator to any of 10 discrete set points. Each set point corresponds to a defined amount of coupling to the power grid or conversely, a certain amount of filtering on the reference output signal. The table below shows the measured accel-tracking sigmas at each control level.

Table 1. Measured accel-tracking sigmas. 162,000 points in each data set.

Control Level	Meas'd Accel-Tr Sigma (s)
0	1.06 e-4
1	5.72 e-5
2	3.06 e-5
3	1.41 e-5
4	7.56 e-6
5	4.04 e-6
6	2.35 e-6
7	1.69 e-6
8	1.43 e-6
9	1.45 e-6

The following two graphs are histograms of the time interval data at levels 0 and 7.

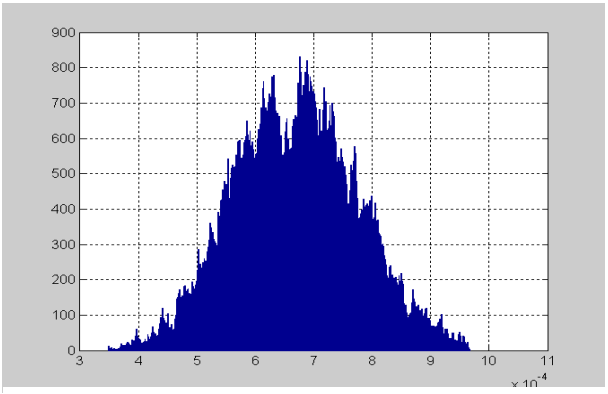

Figure 4. Level 0. Histogram of the time interval between the zero-crossing and reference output signals.

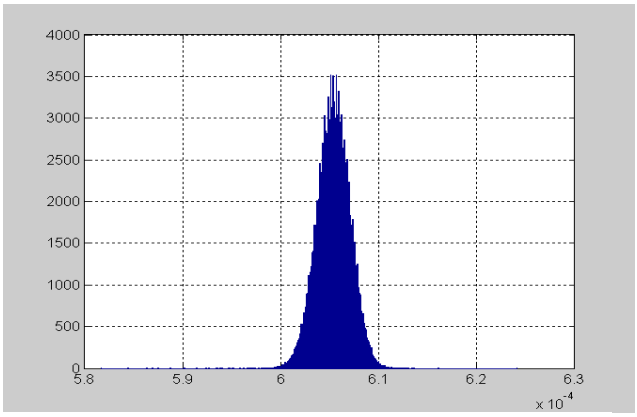

Figure 5. Level 7. Histogram of the time interval between the zero-crossing and reference output signals.

The figures show that when set to a low coupling level of zero, there is a significant amount of reference output wandering with respect to the grid. When set to a higher coupling level of 7, the time interval is much tighter. This also corresponds to slightly more pulse-to-pulse statistical variance.

5 CONCLUSIONS

A programmable phase-locked timing-reference generator has been successfully designed and developed. It allows the user to select an appropriate amount of grid coupling such that performance of both the accelerator and chopper systems is optimized.

The first generation system allowed 10 discrete control levels. The generator has been recently upgraded to incorporate a better digital IIR filter and 100 control points instead of 10.

6 REFERENCES

[1] Nelson, R. O., R. Merl, and C. Rose, "Timing Reference Generators And Chopper Controllers For Neutron Sources," ICANS-XV, 15th Meeting of the International Collaboration on Advanced Neutron Sources, November 6-9, 2000, Tsukuba, Japan.

[2] Rose, C. R., et al., "DSP-Based Timing-Reference Generator User's Guide," LA-UR-01-0419, Los Alamos National Laboratory, Los Alamos, NM 87545.

[3] Rybarcyk, L. J.; Shelley, F.E., Jr., "Improvements to the LANSCE accelerator timing system," 1997 Particle Accelerator Conference, 12-16 May 1997, Vancouver, BC.