CONTROL AND DIAGNOSTIC SYSTEMS FOR THE LNLS 500-MEV BOOSTER SYNCHROTRON

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Abstract

This paper describes the control and diagnostic systems for the new LNLS 500-MeV booster synchrotron. The LNLS Light Source is operated with a home made local controller system (LOCO), using Z80-based CPU modules that run a general software to handle the interface boards. Although the overall structure of the low-level software was unaltered for the LNLS booster synchrotron, time constraints required many tasks previously executed by the high-level software to be transferred to local CPU modules. These modules now make decisions at critical moments in the injection process and the low-level software handles orbit measurement during the energy ramp. A new network board was designed to improve the reliability and speed of the communication between the low- and high-level software.

1 INTRODUCTION

The Brazilian Synchrotron Light Source - LNLS - has started the commissioning of the LNLS 500-MeV booster in late November 2000. Improvements have been implemented in the control system [1] (hardware, low- and high-level control system) in order to respond to new operation needs, especially to control the booster ramping process, the most critical operation.

The CPU speed was increased and a new serial communication interface was developed to reach up to 8 Mbps. The total number of control networks was raised from 9 to 15; the control boards from 350 to 470 and the control points from 3400 to 4070.

The high-level control assigns to low-level control the task to start the detection of the current injected into the booster. Once the energy ramping starts, any change in the ramping speed and the ejection point are handled by the low-level control, configured by the high-level. This is the most significant difference between the energy ramping procedure for the storage ring and the new one for the booster. Orbit measurements during the ramp process are also performed at low level.

Details of these improvements are shown in this article. Details of the commissioning of the LNLS booster are described in [2].

2 HARDWARE

To meet the requirements for the ramping time, the Control Group concentrated efforts on two fronts: the CPU and the communication network. The CPU speed was simply increased from 4 MHz to 8 MHz.

The largest effort was directed to the development of a new serial communication board (Figure 1). The purpose was to increase the transfer rate (up to 8 Mbps, instead of the 2 Mbps still being used for the storage ring) and to improve its efficiency. This new board employs a 87C520 chip (from the 8051 micro-controller family, with special implementations from Dallas Semiconductor).

The major change was to replace the analogic PWM generator by a digital one. With this solution, the new board is more efficient and is no longer affected by thermal drifts.

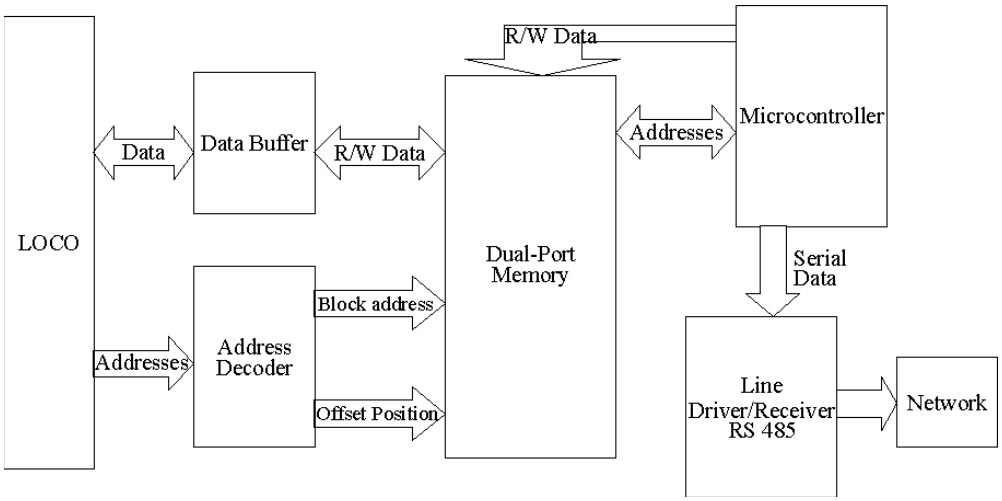

Figure 1 - Block diagram of the new serial board.

The home made electrical interface was replaced with the RS485 Serial Communication standard. For LINAC and storage ring, the networks still use a coaxial cable as the transmission medium, whereas for the booster and transport line twisted pair cable is used.

These measures were enough to satisfy the project requirements of the new injector. Tests are being made to increase the CPU speed up to 16 MHz, if necessary.

3 THE LOW-LEVEL CONTROL

The low-level control software runs in Z80 CPU modules distributed around the facility. As the software system is flexible enough to detect the boards present in the crates, it was decided that this structure should be kept for the booster. It was decided to extend the existing software to do new tasks. The biggest challenge was to define if the control software could respond to the severe time requirements of the processes involved in the operation of the new injector.

The solution was to transfer to the low-level software some tasks previously made at the high level.

One of the most important tasks is the control of the energy ramp. The modules that manage the magnet power supplies receive data tables with the reference voltages like the ramping process in the storage ring. The frequency of synchronism pulses is now controlled at low level due to the short ramping time (1.9 seconds). The complete cycle process takes about 6 seconds.

The parameters for starting, speed changes, ejection time and stopping are transferred to the CPU module that manages the booster synchronism. After receiving the parameters, this CPU module is put in the special state of current detection to determine the moment to start the ramp. The current injected into the booster is read synchronously at each pulse from the main clock generator giving the synchronism to the gun, LINAC and the injection *septa*. The CPU waits a programmable delay between the pulse and the current reading in order to measure the current that is actually captured in the booster.

As soon as the current is above a threshold (one of the previously defined parameters), the CPU module turns off the signal that enables the independent delay generators used for the injection subsystems. At the same time, the booster clock generator is turned on and the CPU modules at the power supplies start to receive the trigger to ramp. The synchronism CPU module counts the number of trigger pulses in order to switch the clock frequency at the predefined moments chosen by the high-level control, as well as to turn on the general ejection signal and to stop the clock.

Large pieces of the general low-level software were rewritten, in order to perform new tasks and deal with the new boards. That was an opportunity to review and optimize the whole original code, leading to improvements that made possible faster ramping processes in the booster modules. Even with the additional implementation, the software size successfully increased by only 10%. This is significant because the software is recorded in an EPROM and has to fit in the 32-Kbyte capacity of the component.

4 THE HIGH-LEVEL CONTROL

Figure 2 shows the window layout in the high-level software used to control the ramping process in the booster synchrotron. In the ramping process of the booster magnet power supplies, the reference values are calculated by the high-level control using configurations selected by the operator (column ***Config*** in Figure 2).

The operator can also set the time to change a stage (Column ***T (ms)***) and the *finesse* (column ***F***) for each stage. All other parameters - initial energy, speed, frequency, energy difference and number of steps in each stage (columns ***E (MeV)***, ***V (MeV/s)***, ***TR (Hz)***, ***DP MeV*** and ***#Passo***) respectively - are calculated by the high-level software. Columns ***TG*** and ***DT*** are the gap voltage and detune of the RF system. Up to 10 stages can be defined.

The operator can select how many steps the boards with 12-bit DA converters should receive to complete the ramp.

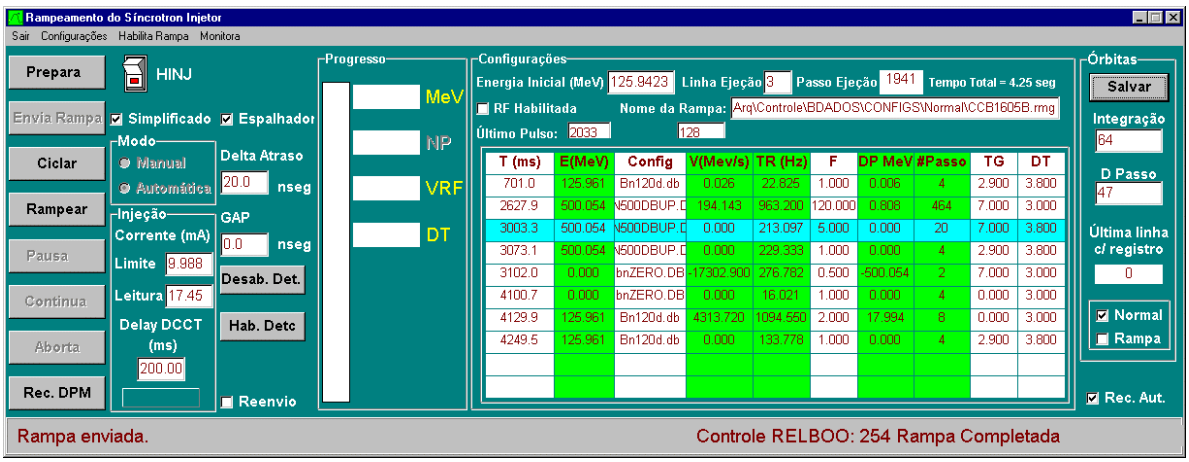

Figure 2 - Layout of the high-level software for the LNLS booster ramping.

The 16-bit DA converter boards are set during the ramp at every pulse from the clock generator, while the 12-bit DA converter boards set a new voltage value to their power supplies every 4 pulses. Both types of board need to do a linear interpolation to make smoother changes of DA output.

Considering the different pulse steps and the interpolation, the number of pulses needed from the clock generator is given by:

$$N_{Pulses} = 16 * N_{Steps12} - 15 \qquad (1),$$

provided this number do satisfy the condition for the 16-bit DA converters:

$$N_{Pulses} = 4 * N_{Steps16} - 3 \qquad (2).$$

The CPU module that manages the booster synchronism reports to the high-level control what stage is in process during the ramp and this information is available to the operator (*Ramp completed*, in our example in Figure 2).

The operator can start the ramping process by clicking a button or by checking a box for automatically starting a new ramp once the previous one is finished (*Automatic* - Figure 2).

The beam from the booster can be injected into the storage ring at different longitudinal positions by checking a box to change the reference delay in the independent delay generator (*Scattering* - Figure 2).

For orbit measurement, the operator can select how many readings should be accumulated, the number of steps between two accumulations and the last stage to be measured. These configurations are used only in the ramping mode.

5 ORBIT MEASUREMENT

The orbit measurement system consists of a set of 12 strip-line beam position monitors (BPM) and 6 Bergoz electronics, each one monitoring a pair of BPMs. There are six CPU modules controlling beam position monitors (BPM) of the booster, each one in charge of only a pair of AD converter boards. The CPU uses these boards to switch monitor electronics and to read both X and Y position values for alternate monitors. The switching time is about 100 ms so that a complete reading of a pair of BPMs takes about 200 ms.

During the ramp process, the values are read and accumulated a certain number of times (set at high level, for averaging) and then stored. These results remain available and are sent continuously to the high level as long as the CPU modules are left in the ramping mode. The synchronization follows from the same trigger signal produced for the energy ramp. As there is room to store up to 20 series of data, the operator can define the number of pulses between two data acquisition processes. This way it is possible to observe how orbit changes along the ramp (Figure 3).

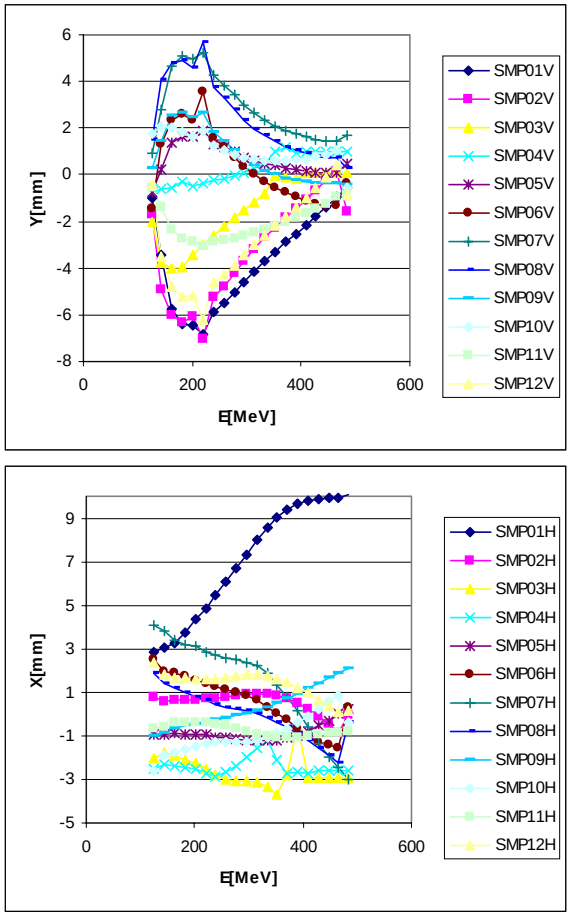

Figure 3 - Horizontal and vertical beams position, at 12 BPM, during a ramp.

6 CONCLUSION

The new Control System for the LNLS 500-MeV booster synchrotron has good performance and reliability. Improvements are under way in order to reduce the time necessary to restart a ramp.

7 ACKNOWLEDGEMENT

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8 REFERENCES

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[2] P. Tavares et al., *Commissioning of the LNLS 500 MeV Booster Synchrotron*, these Proceedings.