UPGRADE OF THE LNLS SYNCHROTRON LIGHT SOURCE TIMING SYSTEM

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Abstract

We describe the theory of operation and the results obtained with the upgrade of the timing system of the LNLS Synchrotron Light Source, developed as a result of the construction of a new 500-MeV booster synchrotron. The system uses ECL logic and differential transmission of the signals through the backplane, which is connected to 11 delay modules that produce the trigger signals necessary for all pulsed hardware in the accelerator facility, including klystron modulators, electron gun, kickers and septa. All trigger signals are synchronized with the coincidence signal of booster and storage ring revolution frequencies. The rms jitter between two delay modules is 200 ps, whereas the rms jitter with respect to the RF waveform is below 20 ps.

1 INTRODUCTION

The LNLS old timing system was capable of producing trigger pulses for all the pulsed devices that were part of the injection process in the storage ring starting from the LINAC. For this process two types of trigger pulses were necessary: with and without pre trigger pulse[1].

The injection system with the new 500-MeV booster synchrotron demanded not only the addition of more hardware to trigger the new pulsed devices, but also the implementation of new protocols for interaction with the control system [1]. Finally, new timing signals, in particular the coincidence signal that connects the revolution frequency of the storage ring to the revolution frequency of the booster synchrotron were added.

The booster synchrotron cycles at a fairly low rate (0.17 Hz) and a sizeable amount of current (at least 15 mA) must be ramped to high energy, in order for the storage ring to be filled with the nominal current (300 mA) in a reasonable time (15 minutes). In order to avoid wasting time in the event of LINAC energy fluctuations, the decision to start ramping is delegated to the low-level control system. The energy ramp begins when the current captured in the booster synchrotron reaches a predetermined threshold. In this procedure, once this threshold has been crossed, and before the energy ramp begins, the control system acts on the timing system through a new command that allows some devices to stop (injection kicker, injection septum and electron gun) while others devices continue pulsing (LINAC klystrons modulators).

When the energy ramp finishes, the control system acts again on the timing system to produce a single clock pulse, synchronized with the coincidence signal. This pulse is used to trigger the booster synchrotron ejection elements (kickers and septa) and storage ring injection elements.

More details about the booster synchrotron operation are given in [2].

[1] These pre-trigger pulses are needed in order to ensure that the pulse forming networks (PFNs) in the high power klystron modulators are properly charged.

2 SYSTEM DESCRIPTION

The LNLS timing system has three layers between the master clock signal (RF signal) and the signals produced to trigger the several pulsed devices (see figure 1)

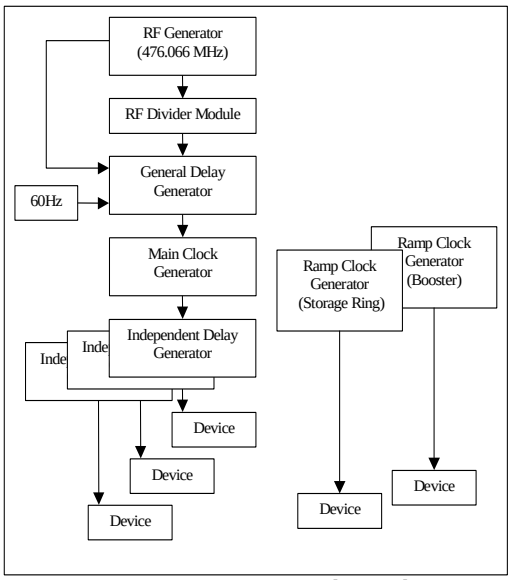

Figure 1: Timing system hierarchy

An RF generator is used to supply the RF system of both accelerators as well as the timing system.

A set of RF dividers is used to produce the booster synchrotron and storage ring revolution frequency signals and the coincidence signal between them (see figure 2).

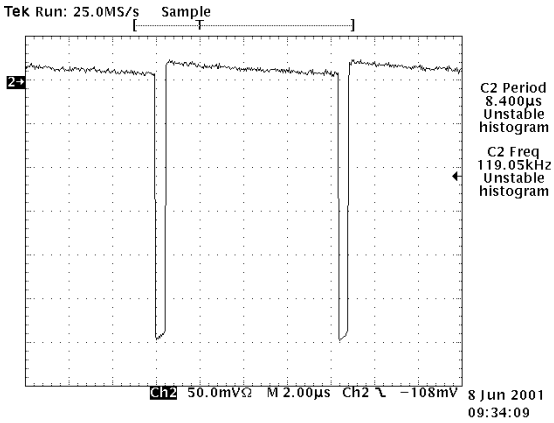

Figure 2: ECL coincidence signal

The revolution frequency and the coincidence signals are generated for instrumentation purposes.

The general delay generator uses the RF signal, coincidence signal and the mains signal to produce 20 MHz and 60 Hz signals, both synchronous with the RF signal. These two signals are used as the time base for the independent delay generators and as the time base for the main clock generator. The general delay generator can adjust a global delay from the coincidence signal in a full range of 7.5 µs and resolutions of 2.1 ns (coarse adjustment) and 20 ps (fine adjustment) in all the independent delay modules.

Referencing the timing signals to the mains signal (60 Hz) is important to minimize the effects of magnet power supply ripple on the bean.

The main clock generator is installed on a 19'' eurocard crate with the 11 independent delay generators and produces three kinds of trigger signals, which are: trigger pulses with and without pre trigger that are generated from the injection rate (1 Hz typical) and ejection trigger pulses generated from the ramping and ejection rate (0.17 Hz). These trigger pulses are transmitted differentially by the backplane using ECL logic levels. This card also drives and provides the 20 MHz ECL differential signal (synchronous with the RF generator) on the backplane.

The independent delay generators use the ECL signals on the backplane as the reference to produce delayed trigger signals for all pulsed devices during de injection or ejection processes. These modules are capable to produce signals with large relative delays (3.2 ms) and with high resolution (200ps).

The ramp clock generators produce the signals that synchronize the ramping devices through interruptions in their local controllers' CPUs.

Table 1: Main parameters of the LNLS timing system

RF frequency	476.066 MHz
Storage ring harmonic number	148
Storage ring revolution period	311 ns
Booster harmonic number	54
Booster revolution period	113 ns
Storage ring and booster coincidence	3996
Coincidence period	8.4 µs
General delay coarse step	2.1 ns
General delay fine step	20 ps
General delay range	7.5 µs
Maximum repetition rate	15 Hz
Minimum repetition rate	0.059 Hz
Number of delay boards (Independent delay generator)	11
Number of delay chanels per delay board	2
Delay boards coarse step	50 ns
Delay boards fine step	200 ps
Delay boards step	3.27 ms
Jitter between two independet chanels	200 ps (rms)
Jitter between any chanel and RF	20 ps (rms)

3 TECHNICAL CHARACTERISTICS

The RF dividers and the general delay generator were built using ECLinPs technology whose components are capable of producing rise and fall times bellow 300 ps [3]. The timing system was concluded before the new ECLinPS Plus series was release (rise and fall times bellow 180 ps).

The main clock generator and the independent delay generators were built using TTL technology, but the timing backplane signals have ECL logical levels (see figure 3).

We used two DC power supplies, one of them a switch mode to provide +5V and another using LM333 negative voltage regulators to provide -5V, -2V, -1.3V and -0.85V.

The independent delay generators besides supplying electrical trigger signals also supply optical trigger signals for the several devices. In the areas that electro-magnetic interference is present (in the proximity of the high power pulsed devices), this system characteristic is very useful.

4 SYSTEM TESTS

The high frequency circuits were carefully designed and interconnected to make sure that the ECL transmission lines match termination. We did not have many problems with the ECL circuits.

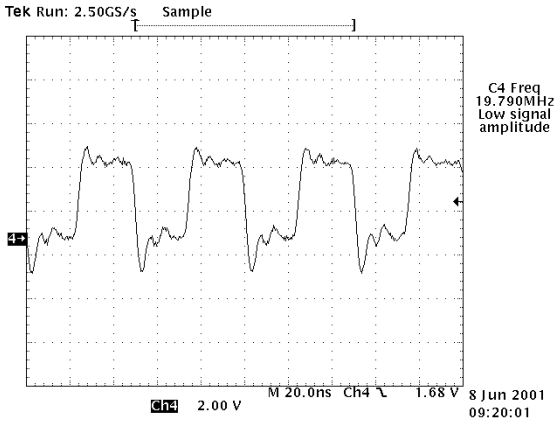

Figure 3: 20MHz signal after ECL to TTL conversion at the last delay board on the backplane

The control system [2] interacts with the timing system through some digital interface cards and mainly through some lines of the backplane (8 data bits, 4 address bits, 16 card identification lines and the Read and Write CPU lines).

The control system cards are installed on a 19 " eurocard crate and timing system cards (main clock generator and independent delay generators) are installed on another 19 " eurocard crate. We joined these two crates with a flat cable that interconnects the lines shared by the two systems and we had some problems for this extended crate:

The interaction among the digital signals through the GND (crossover) and the long tracks caused spurious accesses in some control system cards. Some pull-up resistors in the read and write CPU line, at the end of the control system crate minimized these problems.

The control system uses the 16 identification lines whenever some card is accessed. In the independent delay generators, it was necessary to put a small capacitor (270pF) to GND in these lines to filter fast noises (up than 2V) that appeared in certain circumstances.

Transmitting the differential ECL signals trough the backplane was the most difficult task because in the proximity of the ECL differential lines, there are several TTL digital control system lines. TTL edges induced noise in the ECL lines, certainly because the TTL levels are much higher than ECL levels. We had to put some 560 pF capacitors to the GND in some TTL lines to smooth the TTL edges, in order to decrease the induced noise in the ECL signals.

5 ACKNOWLEDGEMENTS

The timing system would not have been implemented in due time whithout the great help from J. R. Piton and J. G. R. S. Franco.

6 CONCLUSION

The timing system has been in operation since March 2001. The performance parameters of the system meet the new 500-MeV booster synchrotron requirements. In a future version, we will implement the whole system (control and timing system) in the same crate in order that to minimize the integration problems. In order that to decrease the jitter between two trigger signals, we can use ECL logic to implement the main clock generator and the independent delay modules.

5 REFERENCES

[1] J. R. Piton et al., *Control and diagnostic systems for the LNLS 500-MeV booster synchrotron,* these proceedings.

[2] P. Tavares et al., *Commissioning of the LNLS 500-MeV booster synchrotron,* these proceedings.

[3] Motorola High Performance ECLinPs and ECLinPs Lite Data.