A SIMPLE METHOD FOR REAL-TIME DSP-BASED NEUTRON CHOPPER SPEED AND PHASE CONTROL

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Abstract

Spallation-neutron facilities often use precisely-phased rotating choppers to parse the neutron beams that are used in various experiments. Typically, the reference signal is a digital pulse train of nearly-constant frequency. A chopper provides phase and frequency information to a controller by outputting a digital pulse each time its rotating blade passes a top-dead-center (TDC) location. Early controller designs used analog techniques to measure speed and phase and perform the necessary closed-loop control. More recently, purely digital techniques using digital signal processors (DSPs) and counter-based phase detectors have been implemented. This paper describes a relatively simple and low-cost method of implementing chopper speed and phase control with an off-the-shelf DSP card. In this technique, the reference and chopper-TDC digital-pulse trains are slew-rate limited to form trapezoidal waveforms which are sampled by 16-bit ADCs on the DSP board. The DSP finds the zero crossings, computes the frequency and relative phase of the two input signals and performs the dual-loop feedback control functions. A 16-bit DAC outputs a control voltage to a chopper-motor power driver. The paper also describes the rate-limiting circuitry, the real-time dual-loop control algorithm, and system performance.

1 INTRODUCTION

Neutron chopper speed and phase control has been implemented in both digital and analog formats. Within the past 20 years, purely analog controllers measured phase and speed and adjusted the chopper rotation [1]. More recently, digital designs performed this function [2,3]. This paper describes a simple method that is a hybrid between digital and analog techniques of implementing a speed and phase controller using an off-the-shelf DSP card. This method requires that the reference and chopper TDC signals be slightly modified from their digital formats to an analog slew-rated limited version.

This technique is a way of implementing a controller using standard components and requires little custom engineering. It is suitable for all slow T-zero choppers and some higher-speed disk or frame choppers. The paper describes the hardware format of the controller, the theory of operation, and the control algorithm that is used to implement the dual-loop control functions.

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2 HARDWARE

The controller is housed in a 4U-high by 19”-wide rack-mount chassis. A simplified block diagram of the speed and phase controller is shown below in figure 1. In general terms, it consists of an analog card for signal conditioning and some control, a digital card, and an Innovative Integration SBC32 TMS320C32-based DSP card.

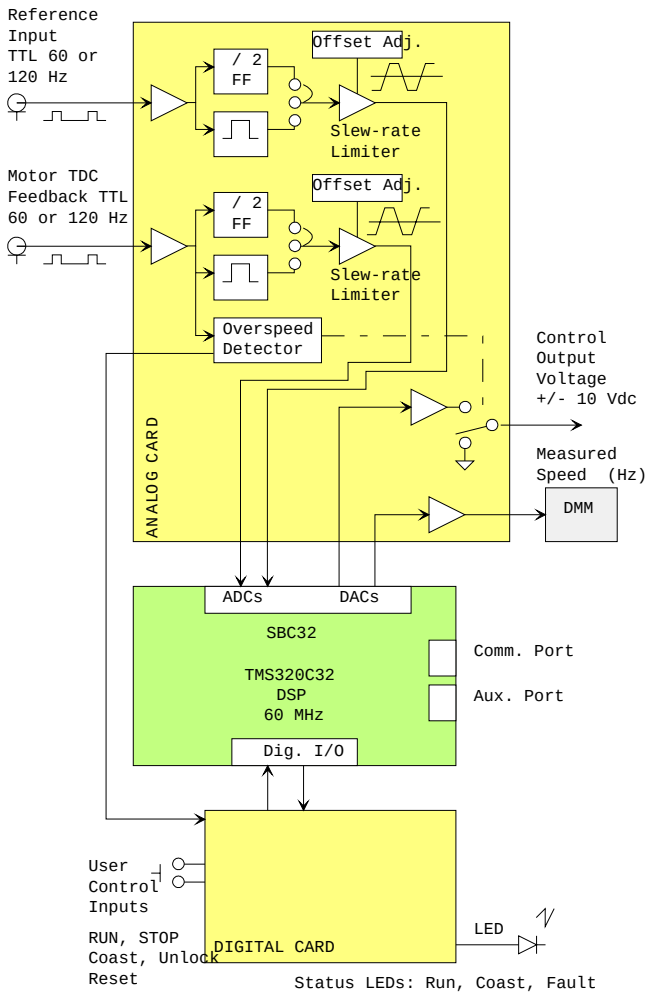

Figure 1. Simplified block diagram of the neutron chopper speed and phase controller.

Referring to figure 1, the analog card has two inputs: one for the reference TTL signal and one for the motor’s TDC feedback signal. Logic buffers then provide these signals to Flip-Flop divide-by-two counters and one-shot

timers. Jumpers allow the user to select the divide-by-two function or the one-shot outputs. Simple OP AMP circuits convert the TTL pulse trains to slew-rate limited analog signals which are fed to the ADCs on the DSP card. The system is designed to accept a nominal 60 or 120 Hz reference but could accept others with minor modifications to the software.

An over speed detector monitors the frequency of the motor and inhibits the control signal using a relay if the speed surpasses a pre-set limit.

Analog control signals from the DSP card are buffered and then sent to the motor power amplifier and a front panel meter for status and monitoring.

The digital card serves largely as a signal pass-through card routing signals from front-panel momentary switches to the DSP card's 16-bit digital I/O port and providing conditioning necessary to drive the status LEDs.

The DSP card uses the 'C32 floating-point DSP and runs at 60 MHz [4]. Referring to figure 1, it has a main serial communication port used for communications with the board, a second port that can be programmed for data I/O, a 16-bit digital I/O port, four 16-bit ADCs and four 16-bit DACs. The board can be programmed to operate using an on-board flash PROM. Upon power-up, it boots and loads the control program from the PROM making a stand-alone speed and phase control system.

The slew-rate limiters are simple OP AMP circuits as shown below in figure 2.

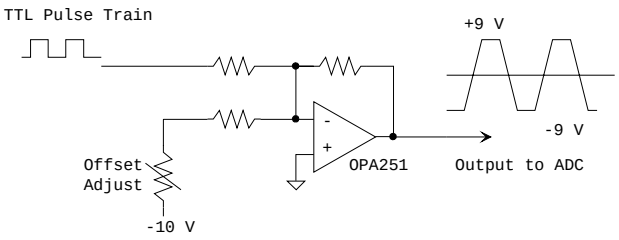

Figure 2. Simplified schematic of a slew-rate limiting circuit.

The OPA251 OP AMP slews at about 0.01 V/μs which provides about 1.7 ms of rise and fall time. The fast rise and fall times of the input TTL signals are converted to trapezoidal shaped signals by the slow OP AMP. At the DSP's 3-kHz sampling rate, it grabs about 5 points per rise and fall. Other more elaborate circuits for accurately controlling the slew rate were considered, but the above circuit has proven to work satisfactorily. An offset adjust potentiometer is available for initial calibration to adjust the positive and negative symmetry of the output waveform, but this is not actually necessary because the relative phase of the reference and motor feedback signals can be adjusted digitally in the control algorithm.

The ADCs have a signal-to-noise ratio of about 72 dB. Using that number and the rise or fall time of the input waveforms, the DSP is able to measure an input signal's period to within about 300 ns.

3 THEORY OF OPERATION

Figure 3 shows the Simulink/MATLAB block diagram of the controller implementing a dual-loop topology. The inner loop controls speed and the outer controls phase. The motor transfer function is shown as a block and incorporated fully as an s-parameter model when simulating the system.

As shown, the velocity loop uses only proportional and integral terms. For the PHAROS T-zero chopper, the proportional term is about 200 and the integral term is about 1.0. The outer, phase loop, is controlled by only a proportional gain term, Kp_ph, which is about 1.0. The DSP samples the incoming waveforms and runs internally at 3 kHz, but the internal control loop runs at the reference rate, about 60 Hz. The two zero-order-hold sampling blocks ensure model integrity at the 60-Hz internal-loop rate.

The integrator and 2π block convert frequency in Hertz to phase in radians.

4 PERFORMANCE

To date, several tests have been done. One was to confirm the slew-rate method as an accurate measurement technique. Data show it is able to measure the frequency of a fixed input signal (60.0000 Hz) to the fourth decimal place confirming the expectation of about 300-ns period uncertainty.

Sample waveforms of input TTL signals and slew-rate limited outputs to ADCs are shown in figure 4. The top trace shows the 60-Hz input and the bottom trace is the slew-rate limited output. The range is from about +9 to –

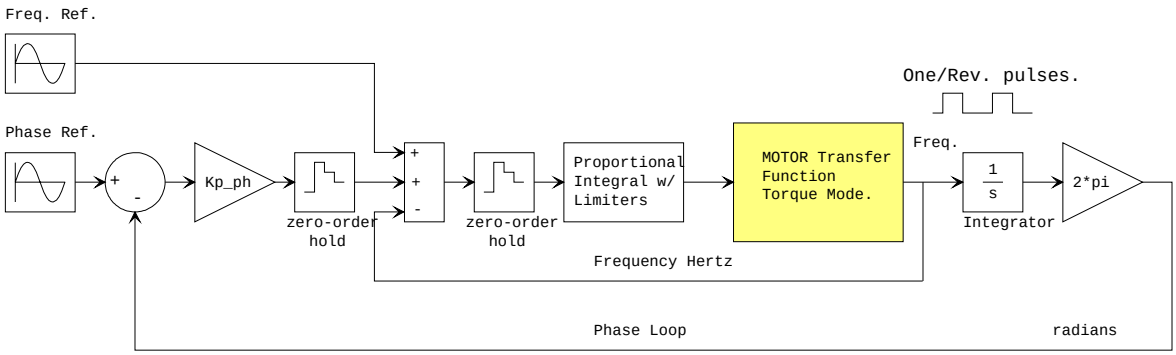

Figure 3. Simulink control-system model of the speed and phase controller.

9 volts with a fall time of about 1.7 ms.

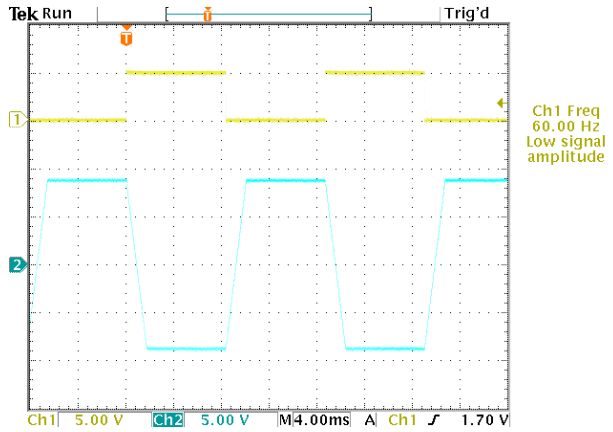

Figure 4. Picture of a TTL input and slew-rate limited output signal. Top: Input TTL signal. Bottom: Slew-rate limited signal ranging from about –9 to +9 volts.

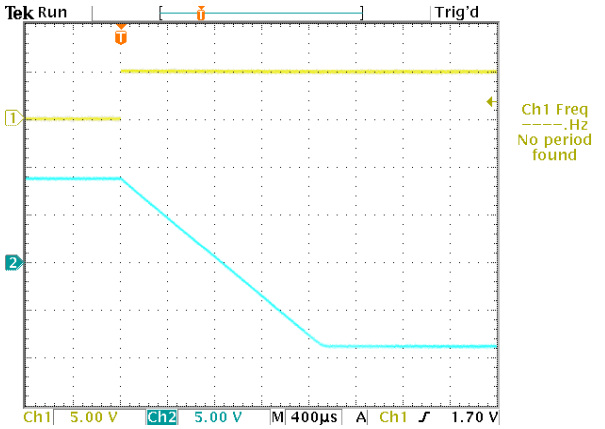

Figure 5. Expanded scale of figure 4. Top: Input TTL signal 0 to ~5 V. Bottom: Slew-rate limited signal showing fall time of about 1.7 ms.

The slew-rate limiters invert the polarity of the TTL input signals, and the DSP is programmed to determine the phase and frequency of the input signals at the negative-sloped zero crossings. This is advantageous when using the one-shot circuits because they have negligible jitter on their rising edges and an unacceptable amount on their falling. Slope doesn't matter when using the flip-flops for frequency division.

The speed and phase controller has been operated with the chopper simulator chassis configured as torque-mode PHAROS T-zero and provided chopper-tracking histograms shown in figures 6 and 7. In figure 6, the timing-reference generator was set to level 2, and in figure 7, it was set to seven. Figure 6 shows a one standard deviation of about 583 ns. Typical numbers ranged from about 500 to 900 ns because of the peregrinations of the timing reference and limited sample size of about 1000 points. The 1.18 µs standard deviation in figure 7 was within the range of about 1 to 1.4 µs.

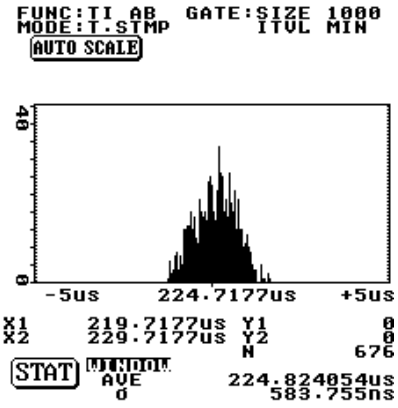

Figure 6. Chopper-tracking histogram of the controller with the chopper simulator. Ref. at level 2.

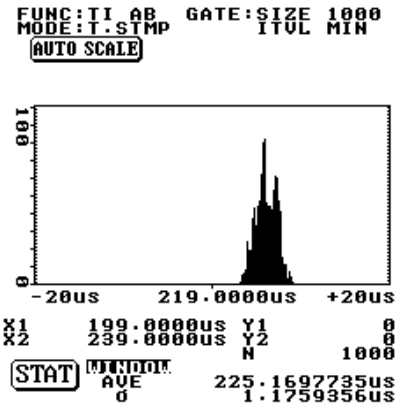

Figure 7. Chopper-tracking histogram of the controller with the chopper simulator. Ref. at level 5.

5 CONCLUSIONS

This chopper speed and phase controller is a simple approach to a difficult problem. It uses off-the-shelf commercial units and simple DSP techniques to accurately control chopper phase and speed.

Additionally, the auxiliary RS-232 port has been successfully used on the local network, via a National Instruments ENET-232/4 ethernet-to-RS232 interface, for remote control of the chopper. Using the remote connection, a user can monitor chopper performance, adjust loop-control parameters, and start and stop the unit.

Additional chopper-tracking data will be taken in coming weeks with actual chopper hardware once it has been balanced and assembled.

6 REFERENCES

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