# BUNCH-BY-BUNCH DIGITAL DAMPERS FOR THE FERMILAB MAIN INJECTOR AND RECYCLER

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*Abstract*

A digital transverse and longitudinal bunch-by-bunch damper has been prototyped and tested. The damper is based on immediate 14-bit digitization at 212 MHz (4x the 53 MHz RF bunch frequency), digital pipelined processing in field-programmable gate array (FPGA) logic, and a digitally synthesized damping kick driven by a 212 MHz DAC. A single board performs all calculations for both transverse and longitudinal damping, as well as providing extensive diagnostic read out, and automatically switching between the variety of beam types present. Initial prototyping was carried out by customizing firmware on a commercial board, and has successfully demonstrated bunch-by-bunch transverse damping, antidamping, and pinging. Longitudinal damping uses identical firmware with different FIR coefficients, and will be beam tested when cavities and power amplifiers are installed in the Main Injector summer 2003. A second generation board, in which damping calculations for all 3 coordinates are performed in a single large FPGA is in fabrication. Several other applications are being considered for this board, including implementation of an entire Low-Level RF system on a single board.

## INTRODUCTION AND MOTIVATION

Fermilab's Run II began without functioning beam dampers on any of its accelerators. Existing dampers had either been decommissioned or were inappropriate for collider mode operations. As a result, a crash program to develop general-purpose dampers using state-of-the art digital techniques was initiated for the Main Injector and Recycler, in addition to specialized dampers for the Tevatron[1-2] and Booster [3].

A main motivation for adopting a digital approach to beam dampers for the Main Injector and Recycler was its flexibility to deal with the wide variety of beam types and operating modes present. Longitudinal and transverse instability and injection dampers were required. Beam types include ramping and stored Antiproton and Proton beams. RF beam structures requiring damping include 53 MHz full batches (1-6 trains of 84 bunches in the h=588 RF system), 53 MHz short batches(5-15 bunches), 53 MHz coalesced bunch, 2.5 MHZ and 7.5 MHZ batches, and DC beam. These modes are interleaved arbitrarily on a cycle-by-cycle basis during Main Injector operations.

Additional operations such as bunch-by-bunch variable gain damping and anti-damping, pinging and noise injection, selective bunch ejection, variation of filter coefficients during the machine ramp, and longitudinal arbitrary RF waveform generation were desired. A "virtual oscilliscope" capability was desired to display signals at various stages of processing. These features can be provided without additional hardware in a system based on digital processing with large-scale programmable logic.

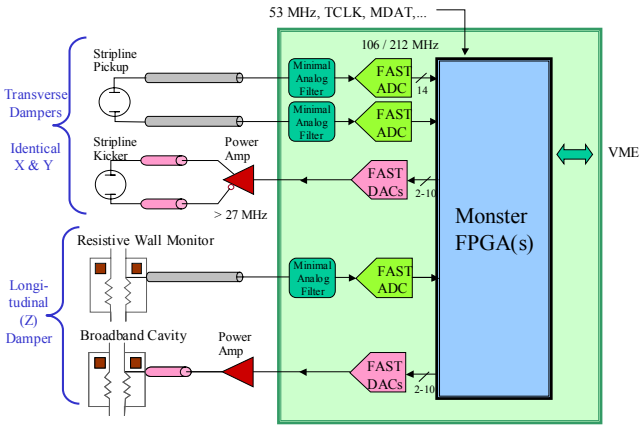


Figure 1: Three-coordinate Digital Damper. Signals on cables from the tunnel are immediately digitized, processed with bunch-by-bunch multi-turn digital filters in a large Field-Programmable Gate Array (FPGA), and the digitally calculated kick is sent through a DAC to the power amplifier and transverse or longitudinal kicker.

## DIGITIZATION RATES

A fundamental design decision is the required ADC conversion rate. We have chosen 4x the RF bunch frequency. This represents the minimum digitization rate needed to capture a bunch-by-bunch amplitude and phase, while rejecting DC and closed-orbit offsets. In the frequency domain, this permits reconstruction of the In-phase and Quadrature (I&Q) components at the RF carrier frequency with simple 2-point sample differences. See figs. 2-4.

The minimum DAC update rate for a bunch-by-bunch damper is equal to the RF frequency. However, we have found it advantageous to have a DAC update rate 4x (and eventually 8x) the bunch frequency, driven by an up-sampling FIR. This permits digitally fine-tuning the kick timing, sculpting the drive waveform to correct for analog defects in the power amplifier and cables, and kicking the beam at frequencies above baseband [3].

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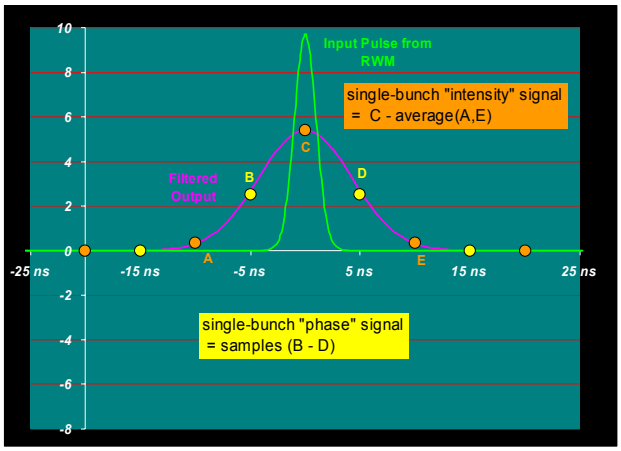


Figure 2 – Single bunch sampling of a unipolar Wall Current Monitor (WCM) signal with four 212 MHz samples per 53 MHz bunch. A 70 MHz low pass "anti-aliasing" filter spreads the pulse +/- 5 ns in time so the ADC will not miss the bunch signal. The filter's suppression of the sharp 1-2 ns peak from theWCM signal also reduces the dynamic range required from the ADC. The bunch amplitude is obtained from the 3-point difference of samples (C-average of (A,E)). The bunch phase is obtained from the 2-point difference (B-D) .

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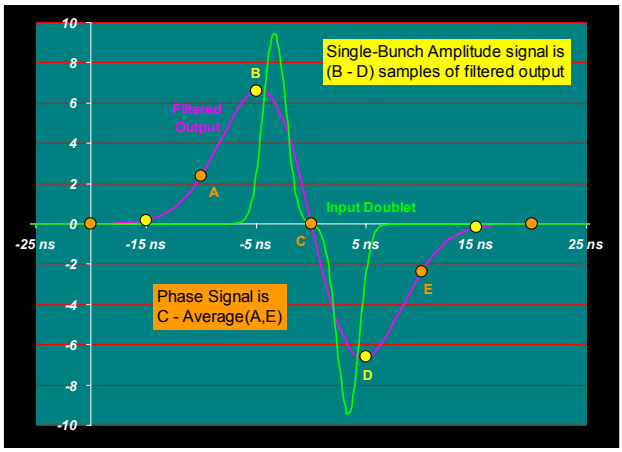


Figure 3 – Single bunch sampling of bipolar doublet at 4 samples/bunch. The situation is identical to unipolar sampling except that the roles of the Amplitude and Phase signals are reversed.

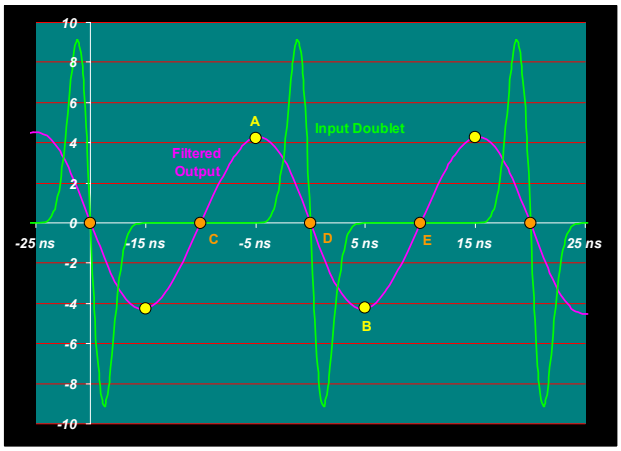


Figure 4 – Single bunch sampling of repetitive bunch train. Although the filtered signal resembles a sine wave, it actually contains bunch-by-bunch phase and amplitude information.

## PROTOTYPE HARDWARE

The prototype hardware (figure 5) uses an Echotek ECDR-814X-AD card with 8 channels of 14-bit 106 MHz digitization (interleaved to provide four channels of 212 MHz sampling), a 212 MHz DAC daughtercard, a VME-64 crate with Power-PC readout processor, and an interface box containing filters, buffer amplifiers, signal splitters, and delay cables.

Figure 5 – Prototype hardware VME Crate and interface.

The longitudinal damper input signal is the phase signal from a wall current monitor, digitized as shown in fig. 2. The transverse damper signal is derived from the difference output of hybrid transformer connected to a stripline pickup. The position signal is a bipolar signal with amplitude proportional to the bunch position, digitized as in figures 3 & 4. One pickup is used in each coordinate. All signals go through a low-pass filter (Mini-Circuits BLP-70) and buffer amplifiers for overload protection and signal termination. They are then resistively split into two ADC channels, with one channel delayed by ~5ns to obtain 212 MHz interleaved sampling.

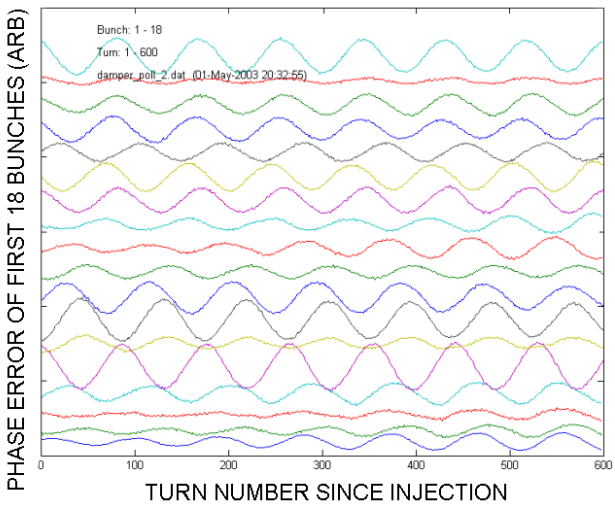


Fig. 6 – Bunch-by-bunch phase measurements with the Main Injector Damper, showing bunches executing synchrotron oscillations due to individual phase and energy errors present in beam delivered from the Booster.

An online display was generated by a MATLAB application which can display bunch-by-bunch amplitude, phase, tune, raw ADC or digitally filtered data or the applied kick. Data can be displayed for single bunches or as a function of bunch number or turn number.

### *Digital Filter Algorithms*

Transverse and longitudinal filters use identical firmware with different FIR filter coefficients. The transverse damper is a digitally pipelined 3-turn filter similar to ref. [3]. The transverse kick for each bunch is calculated as the weighted sum of the transverse bunch positions measured on the previous turns (a 3-turn FIR filter). The three weights are uniquely determined by the system gain, the machine tune and the betatron phases at the pickups and kicker, and the fact that the weights must sum to zero in order to reject closed orbit distortion.

The longitudinal kick to each bunch is proportional to the rate of change of the phase of that bunch. This derivative is calculated by taking the weighted sum of the phase measurements made on the last 8 turns (an 8-turn FIR filter). The eight FIR weights are given by a linear ramp passing through zero between the 4$^{th}$ and 5$^{th}$ bunch. This choice of weights rejects DC phase offsets and is mathematically equivalent to a least-squares fit to the slope of the phase on the last 8 turns.

## BEAM TEST RESULTS

The transverse damper took advantage of existing stripline pickups and kickers, and worked essentially as soon as the firmware was completed (see figure 7).

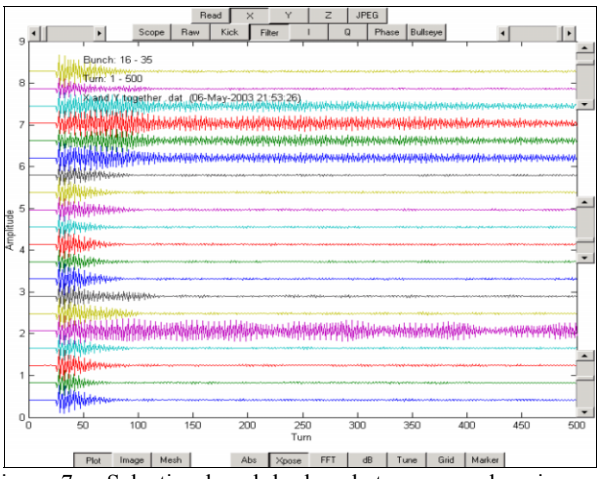


Figure 7 – Selective bunch-by-bunch transverse damping and anti-damping of 53 MHz bunches for the first 600 turns in the Main Injector. Each trace represents the turn-by-turn position of a single bunch. All bunches were damped except the group of four near the top (which were left alone), and the single bunch near the bottom (which was antidamped and eventually ejected).

The selective transverse antidamping or pinging of bunches (fig. 7,8) was straightforward to implement in the FPGA firmware. This opens up possibilities for tailoring the bunch structure and offers the amusing possibility of neutrino communications.


Figure 8 – Selective ejection of bunches from an 84-bunch batch during acceleration in the Main Injector.

Longitudinal damping digital filters have been tested with beam and perform as expected. Actual tests of longitudinal damping await the installation of broadband damping cavities and amplifiers currently scheduled for August 2003.

## FUTURE PLANS

A second generation card has been built and will be tested soon. Damping calculations for all three coordinates are performed on a single large FPGA (Altera EP1S25F672C6) instead of the 5 smaller FPGAs on the prototype card. Four channels of 212 MHz ADCs avoids the need for interleaving 106 MHz digitizers. D/A conversion is performed by four 424 MHz DACs, which will allow "sculpting" the kicker output waveform to correct for analog defects in the power amps and cables. The system will be packaged as a standalone (NIM) module with an Ethernet interface, thereby eliminating the VME crate, backplane, and readout CPU.

It is clear that the general approach of immediate high speed digitization and FPGA processing has a number of other potential applications in accelerator instrumentation and LLRF control. The large number of high performance PLLs on modern FPGAs opens up additional possibilities. Some applications that we are considering are: beam loading compensation, beam position monitors, beam stacking manipulations using broadband RF systems, and possibly the complete replacement of the LLRF system for the FNAL Booster with the single card developed for dampers.

## REFERENCES

[1] C. Y. Tan and J. Steimel, "The Tevatron Bunch-by-Bunch Longitudinal Dampers", PAC'03.

[2] W. A. Pellico and D. Wildman, "Booster's Coupled Bunch Damper Upgrade", PAC'03.

[3] Klute, Kohaupt et. al., "The Transverse Damping System with PLL Tune Measurement for HERA P", EPAC'96.