BEAM POSITION MONITOR SYSTEMS FOR THE SNS LINAC*

J. Power[†], L. Day, M. Plum, M. Stettler

Los Alamos National Laboratory, Los Alamos, NM 87545

Abstract

The 402.5- and 805-MHz beam position and phase monitors for the Spallation Neutron Source linac are based on standard PC technology. The SNS beam is to be injected into a storage ring with a 1-MHz circulation frequency requiring 650-ns-long minipulses. The injection cycle takes 1 ms and the machine can run at rates up to a 60 Hz. The rf input signals are down converted to 50 MHz and sampled at 40 MHz with 14-bit ADCs to produce I and Q data streams. A custom PCI module has been designed to accept modular digital front end (DFE) and analog front end (AFE) circuit cards. This hardware is installed in a standard rack-mounted 1U computer chassis running Windows® 2000, LabVIEW® and custom DLL software. The system continuously self-calibrates by generating 300-ns long rf pulses which are switched between the AFE inputs and the cables going to the BPM pickups. This provides a TDR-like calibration of the entire system. The system is designed to provide a position and phase resolution of 0.1% of the beam pipe aperture and 0.1 degrees RMS respectively over a 50 µs period. The design of the system is described as well as the initial performance measuring beam during the commissioning of the SNS MEBT.

INTRODUCTION

One of the primary design principals of the SNS linac BPM system was to take advantage of mainstream solution. Another design choice was to make the hardware platform modular to simplify the design and testing as well as to provide a more general purpose instrumentation platform for other diagnostics such as beam current monitors.

We chose to build a PCI carrier card which accepts several plug-on modules including an AFE, DFE and clock multiplier. All analog connections are made through the AFE, via patch cables to the back panel of a generic 1U server PC. The timing and trigger signals attach to the standard front panel of the PCI card.

The instrument is a stand-alone device, providing the capability to serve beam position and beam phase measurements over Ethernet without any external controls requirements. In our case data is served via channel access for compatibility with the SNS EPICS-based control system. For the general case the data can be served to any web browser via the standard LabVIEW® tools. This mode is particularly useful for system testing.

ELECTRONICS

The BPM system operates by down converting the four individual BPM lobe signals which are either 402.5 MHz or 805 MHz to an IF of 50 MHz. These IF signals are sampled at 40 MHz to generate the quadrature information that is processed to measure position and phase. The PCI card that accomplishes the more interesting parts of this process is shown in Figure 1.

Figure 1. The BPM system PCI card showing the clock multiplier (top left), DFE (center) and AFE (right).

industry standard components and software. Using standard PCs running a Windows® operating system and LabVIEW® instrument software was the obvious

Analog Front End

The AFEs used by SNS were designed and built by Bergoz Instrumentation [1] to our specifications. This module, shown on the right end of the PCI card in Fig. 1, contains four channels of down conversion, a local oscillator distribution chain, and a calibration system.

The calibration is made possible by fast-switching networks on the inputs to each down converter channel. A calibration signal, at the same frequency as the beam signals, can be switched to either the input to the down converter, or to the cable connected to the AFE input. The third switched condition is the normal operation one in which the AFE inputs are connected directly to the down converter inputs.

The technique is basically the same as a time domain reflectometer (TDR), except we use a rf burst instead of a step function. This is made possible by using rather long cables between the AFE and the BPM pickups, and by using pickups that have the downstream end of each lobe shorted.
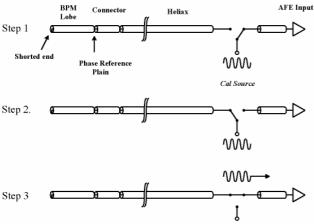

Figure 2. The calibration uses an rf burst to calibrate the down converter chain in step 1, launch a calibration burst down the BPM Heliax cable in step 2 and measure the reflected burst in step 3.

The first step in the process is to inject a rf burst into the input of a down converter channel and measure the amplitude and phase of the result. Next is to launch a burst of the same amplitude into the cable connected to the AFE input. This cable has a round-trip transit time of 300 ns, which determines the maximum length of the calibration burst. This burst reflects off of the shorted end of the pick-up and returns to the down converter input, which is switched in at the time of arrival of the reflected pulse. Having measured the amplitude and phase of the reflected pulse, one has enough information to calibrate the system in amplitude and phase through the entire signal path.

The AFE calibrator circuit is carefully adjusted to give the same amplitude and phase of calibration bursts to each channel by tweaking a resistive splitter on the AFE circuit board.

Digital Front End

The DFE has four channels of 14-bit ADCs clocked at 40 MSPS (see Fig. 1). Filters before the ADCs limit the analog bandwidth to about ±10 MHz. Two FPGAs each process the data from two ADCs to de-convolve the multiplexed quadrature steam created by under-sampling the input at 1.25 times the input period, creating

individual arrays of in-phase and quadrature-phase (I &Q) data. A total of 8 arrays are thus created for the four input channels.

These same FPGAs serve as multiplexers such that raw data and from the ADCs, or preset ramp data may be passed through for testing and de-bugging, instead of the I and Q streams.

A third FPGA is used to generated the timing signals which drive the switches on the front of the AFE for calibration purposes, as well as control the analog gain of the AFE, either 1X or 4X.

PCI Motherboard

The PCI motherboard card is the backbone of our custom hardware. The AFE plugs into the DFE, and the DFE plugs onto the PCI card. The PCI card has eight 256-kB FIFOs, one for each array of data from the DFE. This provides for up to 3.2 ms of data history to be stored for each channel.

One large gate array provides the PCI interface, DMA data transfer for the FIFOs to the PCs memory, timing controls, and a custom 12-bit "L-bus" for control of the DFE.

Three separate power supplies/regulators reside on the PCI card for providing low-noise power to the peripheral modules.

A third clock-multiplier module also plugs onto the top-left corner of the card to generate the differential ADC clocks. This module multiplies the external phase reference of 2.5 MHz up to the required 40 MHz sampling rate. The PLL is serially-programmed to accommodate future reference frequencies such as 10 MHz. The circuit design is based on a LBNL design done by L. Doolittle[2] for their SNS LLRF control systems.

Instrument Packaging

The PCI motherboard and its associated daughter cards are installed in a 1U rack-mounted computer chassis (see Fig. 3). A bracket containing SMA feed-through connectors for the four pick-up lobe inputs, LO drive and calibration drive is attached to the back of the chassis.

Figure 3. The SNS linac BPM system in a 1U, rack-mounted PC configuration.

The phase reference and trigger signals attach via LEMO® connectors of the PCI card panel.

Additional versions of the BPM instrument have been assembled using a 2U rack-mount chassis, which can accept an additional PCI timing receiver card. This is required for the final SNS facility implementation which uses a complex timing system using both VME and PCI hardware.

PERFORMANCE

Nine BPM systems are currently installed and operational at the SNS facility. Six of the units are prototypes which were used to commission the accelerator front end both at LBNL over a year ago and again at ORNL this year. Three systems are improved, second generation hardware, which will be used for commissioning the first DTL tank shortly.

Performance as Installed

For the SNS linac commissioning, we define the measurement resolutions based on minimum beam pulses of 50 μs, meaning we average all data for this duration. With this in mind, we ran the new BPM systems as installed, taking data for the equivalent of 1000 beam pulses over about two minutes. This data was analyzed to determine the phase resolution of the measurement.

As installed, the newer systems provide a position measurement resolution of better than 0.1% of the beam pipe radius, and a phase resolution of about 0.6 degrees rms. Figure 3 shows the phase data accumulated in a typical run, from which the RMS measurement resolution is calculated.
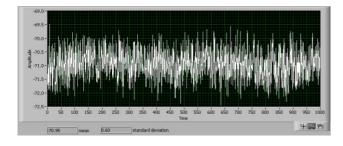

Fig. 3. Data from the equivalent of 1000 beam pulses of 50-μs duration. The phase resolution is calculated as 0.6 degrees.

Frequency-domain analysis of the amplitude measurement data for a single lobe-channel gives a SFDR of over 70 dB as measured on the bench (see Fig. 4).
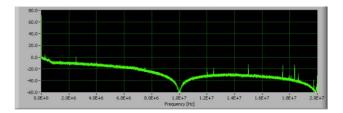

Figure 4. Results of a FFT on 4000 consecutive samples of the amplitude measurement for a single BPM lobe channel. The vertical axis is in db, with 76 being full scale for the ADCs. The horizontal axis is frequency in Hz. The usable dynamic range is about 65 dB.

Issues Needing Further Study

The position-measurement-resolution of the newer systems meets our requirement, but the phase-measurement resolution is not as good as we would like. We currently have a factor of about six higher than our goal. There are technical means of improvement that are being pursued

The phase resolution is primarily a measure of the ADC sampling clock jitter relative to the various rf sources in the system. These include the calibration source, LO source and system reference. Our 0.6-degree resolution is equivalent to 4.2 ns of clock jitter over a bandwidth of a few milli-Hertz to 40 MHz. The high frequency jitter (over 10 kHz) of our clock multiplier VCXO is specified as 1 ns, and substantially lower frequencies are within the PLL loop bandwidth and should be removed. Further study of the jitter of all of our sources is an on-going endeavor.

One expected improvement will be to increase the reference frequency from 2.5 MHz to 10 MHz. We currently use the 2.5 MHz as a hold-over from earlier requirements.

CONCLUSION

We have developed stand-alone beam position and phase measurement instruments based on standard PC hardware and software, with custom-designed PCI cards. The instruments are capable of being communicated with over Ethernet via either EPICS channel access or standard Web browser interfaces. We have achieved a position resolutions of better than 0.1% of the pipe radius and phase resolutions of 0.6 degrees. Further improvement of the phase measurement resolution is being studied.

REFERENCES

[1] Bergoz Instrumentation, http://www.bergoz.com
[2] Private communication with L. Doolittle, ldoolitt@recycle.lbl.gov