PLC AND LINUX BASED CONTROL SYSTEM FOR THE CAMD LINAC

P. Jines, E. Anzalone, B. Craft, A. Crappell, M. Fedurin, T. Miller, M. Smith, Y. Wang, and T. Zhao CAMD, Baton Rouge, LA, USA

Abstract

Louisiana State University Center for Advanced Microstructures and Devices (CAMD) began operations in the fall of 1992. At the time, the facility had separate control systems for the storage ring and Linac. In 1997, CAMD began a control system upgrade project with the goal of producing a single unified control system running on the PC/Linux platform. After completion of the storage ring control system, the Linac control system was designed utilizing AutomationDirect.com PLCs for the real-time components, and PC/Linux for the user interface. The new Linac control system has been completed, and has been operational since July 2002. This paper will discuss the objectives, design, and future upgrade plans for the Linac control system, as well as the experiences with replacing the CGR-MeV VME/OS/9 control system with a PLC/PC/Linux based system.

INTRODUCTION

Efforts to integrate the VME/OS/9 based CGR-MeV Linac control system with the storage ring control system had been difficult. Though OS/9 provided basic TCP/IP capabilities, the third-party control software consumed essentially 100% of the available CPU. Pinging the Linac control system resulted in the expiration of watchdog timers, which in turn lead to a shutdown of the Linac.

The largest problem with maintenance of the system involved documentation and spares. Many components in the system were undocumented or unidentifiable. Efforts to reverse engineer the system had not been successful. Reliability of the system had also become a concern. The components were almost ten years old, and were starting to fail on a regular basis. Luckily, most failures were in known components. However, the sense of impending failure of one of the undocumented or unidentified components forced the control system upgrade to become high priority. Given the inability to reverse engineer these components, CAMD decided to replace the control system instead of attempting to upgrade or integrate it.

The existing VME system was based on a VME computer with custom I/O components. A custom scanner card in the VME crate communicated with the I/O cards via a 50-pin ribbon cable using an in-house protocol. Each I/O card was homogenous in that all digital I/O was a TTL signal, and all analog I/O utilized a 0-10V signal. The cards had a ribbon cable connector on one side, and connected to a 3U Eurocard backplane that handled all incoming and outgoing control signals. The backplane then connected to any signal specific hardware necessary, such as TTL to 24V contact relays or voltage to frequency converters. As all I/O was homogenous at

the Eurocard backplane, this was the point at which the conversion from the old control system to the new PLC system would take place. Special cables were fabricated to connect D-shell DIN-rail breakout boxes to the 96-pin backplane connectors. Using this setup, the new control system could be tested, and the Linac could be reverted to the old control system simply by removing the adapter cables, and reinserting the I/O cards as before.

The timing system was based on yet another undocumented VME card, which provided fiber optic outputs. The source code did not provide a clear description of how the timing was set, so the timing charts had to be measured externally. However, as with the Eurocard backplane connectors, this provided the ideal place to insert the new timing system controls.

HARDWARE DESIGN

The system was architected to be fully distributed so that performance problems could be easily addressed, and additional channels could be added quickly (see Figure 1). The heart of the architecture was separating the interlock code from the code that checked analog signal conditions.



Figure 1: Linac Control System Architecture

One PLC is dedicated to reading analog signals and comparing them against downloaded upper and lower limits. Out of limit conditions are indicated by a digital signal. An input signal is provided that can enable or disable checking of a channel so that an out-of-range condition is not generated if the device is simply turned off as opposed to faulted. With this scheme, performance of the analog limit checking system can be enhanced by splitting the channels into more CPUs as opposed to a single CPU, and the change would be transparent to the rest of the system. Communication with the user interface PC is done thru dual-port memory provided by the H4-ECOM ethernet interfaces. The second PLC is dedicated to the interlock and control tasks. User requests to turn devices on are inputs to this PLC. If all interlocks and analog signal conditions are met, this PLC does the actual turn on. In the event of a linac problem, it turns off the required devices and latches the fault condition. Ramping of devices is also performed by this PLC. As with the analog PLC, the user interface PC sends commands and receives status information via ethernet.

A third PLC provides control and readback of any signals which are not involved in equipment protection or interlock functions. This PLC has no CPU, but provides only a "dumb" interface directly from ethernet to the I/O.

The timing system consists of Stanford Research Systems DG535 Digital Delay/Pulse Generators, with pulses being converted from TTL to fiber by a dedicated chassis. This conversion system either permits or disables pulses based on input from the interlock PLC.

Lastly, all system digital outputs and permits are fed thru an external watchdog system. This system monitors clock outputs from both the analog limit PLC and the interlock PLC, and will turn off all outputs and permits in the event of the failure of either PLC.

SOFTWARE DESIGN

The CAMD storage ring control system provides a device independent applications programming interface where device specific parameters are stored in a PostgreSQL database [1][2]. Device support for both CPU and EBC based AutomationDirect PLCs and SRS devices were already provided in this system[3]. Therefore, to accommodate the Linac control system at the raw device level, only updates to the database were required.

Individual parameter control was accomplished using the ring control system's generic "magnet pages". These pages utilize channel name patterns to configure the windows. Given a list of "magnet" names, the code searches the database for setpoint, readback, shunt, and on/off channels, and configures the window and code accordingly. To accommodate the Linac, this code needed to be extended to handle upper limit, lower limit, out of range indicators, and alternate names for setpoints and readbacks.

To minimize operator training on the new system, the approach chosen for the main user interface was to "clone" the existing CGR-MeV interface as closely as possible, with a few exceptions (see Figure 2). The original interface provided an "on/off/reset" view of each major Linac subsystem. Only one button from the list of "on", "off", or "reset" was active at any given time. An "off" button of either green or yellow would distinguish between "off/enabled" and "off/disabled" conditions. Buttons would flash to indicate on, off, or reset "in progress" conditions. Buttons, as well as all related parameters on the parameter pages, would turn red on fault conditions.

			LINAC	- CON	TROL GUI				
Interlock Display					LINAC Control				
MOD 1 AND 2 KEY	NOK	COOLING R	DY	OK	INIT		OFF	RESET	VIE
GROUNDING 1 RDY	NOK	MOD ANC CAB RDY MOD 1 HEAT RDY MOD 1 HEAT RDY MOD 2 HEAT RDY MOD HV PS RDY KLYS FOC PS RDY KLYS FOC PS RDY GUN HV PS RDY		OK	COOLING		OFF	RESET	VIE
GROUNDING 2 RDY	NOK			OK OK NOK	MOD ANC		OFF	RESET	VIEN
MOD 1 SECU RDY	ок							The Great	
MOD 2 SECU RDY	ок				KLYS_FOC		OFF	RESET	VIE
MOD 1 OIL LEVEL	OK			OK	BEAM_FOC		OFF	RESET	VIE
MOD 1 SF6 PRESS	OK			OK	HF_ANC		OFF	RESET	VIE
MOD 2 SF6 PRESS	ок			NOK	500MHZ		OFF	RESET	VIE
HF AMPL RDY	OK	SUUMHZ AMPL	RDY	UK	GUN_ANC		OFF	RESET	VIE
	VALVE D	isplay					e		
VALVE 1	PEN	CLOSE V		V					
VALVE 2	PEN	CLOSE	VIEW	v	MOD_HVPS	ON	011	RESET	AIEA
	PEN	CLOSE	VIEW		GUN_HVPS	ON	OFF	RESET	VIE
LIN	AC PULS	E Display	VILV		MOD_RUN	ON	OFF	RESET	VIE
MODHV_PS BUNCHER_DEPTH S2 DEPTH		EDIT		GUN_RUN	ON	OFF	RESET	VIE	
		EDIT		-1	HF	ON	OFF	RESET	VIE
				-1	REAM	ON	OFF	RESET	VIE

Figure 2: Control System User Interface

While most features of the CGR-MeV interface were kept, some were changed. In the original system, the operator was required to switch between two or three pages to operate the Linac. In the new system, a single window is utilized. A limitation of the original system is that when a fault occurred, the operator had to search thru several pages to find the analog signal that caused the fault. In the new system, the signals are grouped by which ones are utilized by a subsystem's interlock logic. So, if a certain subsystem is faulted, a "View" button launches a window which shows the status of all signals which are related to that subsystem and could cause the fault condition. For subsystems with longer timeouts and warm-up periods, countdown timers were added. One last enhancement to the system involves operator access to parameters such as upper and lower limits, and notcommonly-used parameters. Global access to these parameters resulted in wildly varying linac tunings, and some limits being so large as to be ineffective. Now, these parameters are only available on "Linac Expert" pages, and are under configuration management control.

INSTALLATION AND COMMISSIONING

While the initial shutdown for installation of the Linac control system was planned for one week, most of which was dedicated to ring vacuum activities. To test the Linac with beam required Radiation Interlock System permits that could only be given when the storage ring was searched and secured. This left about three days to commission the new control system with all interlocks in place. To accommodate this schedule, all components of the system had to be tested before the shutdown, leaving only final integration tasks until the last minute.

The first task was to identify all operating voltages and voltage ranges, so that in the event of a control system failure, a known "electrical" state could be recreated. Next was to test the TTL-to-fiber interface, and to verify that the Linac would operate using SRS pulse generators. Since operation of the old and new control systems simultaneously was not possible, this required the "human interlock" approach.

Analog limit checking PLCs were tested channel by channel, with both upper and lower limits, along with

parameter pages and database entries. Documentation and wiring lists were verified as part of this task.

Analog and digital control of the Linac was verified in one of two modes. First, the old control system would be "in charge" of the interlocks, and the new system would "steal" as many signals as were possible. Secondly, the old control system would not be used, and the new control system would rely heavily on the "human interlock" approach.

Finally, by the first day of the shutdown, all systems except the interlock PLC had been verified. As luck would have it, this was the day that the old system finally crashed. Without the option to reverting to the old system, the first days of the shutdown were spent on Linac controls which did not require ring security. Most of the problems encountered were of one of two forms: timing issues or externally disabled hardware.

Timing issues were the first major problem encountered. The solutions were mainly tradeoffs between the length of time waiting for a system to reach a steady state, and how soon to assume it was broken and engage the interlock code.

Most other problems were caused by a history of being unfamiliar with the old Linac control system. Due to the sensitivity of the code, the lack of documentation, and the criticality of the system, no changes had ever been made by CAMD staff to the system. If the system needed to be changed in any way, it was either done by widening the analog limits to almost full scale or "jumpering out" external relays. This led to a large number of disabled interlocks, or systems whose real status was "faked" as far as the computer was concerned. While most of the first steps in the Linac turn-on sequence had "faked" inputs, the decision was made to write and test the interlock code as written, so that minimal changes would be required later on when the external problems would be properly fixed and the jumpers removed.

In addition to providing interlocks that verified that systems were on and operating properly, we also identified the requirement to check that systems are actually "off". In addition to externally jumpered signals, we also discovered that the "pull up" and "pull down" status of many signals were incorrect. Bad connections or failed relays caused many conditions to appear as acceptable when, in fact, they were not. Consequently, for the next revision of the design, an extensive review of the electrical signals between the PLC and the devices will be required. Also, alarm capabilities that indicate that "off" commands were sent, but the device is still "on" will be required.

The Linac controls which required ring security were straightforward. The timing system had already been tested with the old system, so the testing was mainly an exercise in determining the proper timing for the warm-up vs. interlock. Scope traces and analog voltages were compared against similar values from the old system as commissioning proceeded, so only mild optimization of the pulses, timing, and setpoints were required in later stages. Finally, six days into the shutdown, we had Linac beam injected into the storage ring, and were able to begin recommissioning the storage ring after the vacuum intrusion.

RESULTS AND FUTURE PLANS

The performance of the PLC control system is on target. The goal is to detect faults in time to stop the next Linac pulse, occurring at a 10Hz rate. After analyzing the running system, the Interlock and Analog Limit PLCs have average scan times of 12ms and 63ms. The F4-SDN modules provide a real-time network with a transmission time of 32ms, producing a total average time of 107ms. In the scope of the project, these timings were considered adequate for the first phase. Future upgrades could significantly improve this number by upgrading the Analog Limit PLC architecture from a one CPU, two expansion base model to a three independent CPU model.

The PLC system was "spliced in" at a homogenous, standard electrical interface that provided easy integration and the ability to switch back and forth between the old and new systems for testing. However, this method exposed several limitations in the rest of the Linac tunnel, such as hardwired status signals, jumpered out relays, and incorrect "pull up" and "pull down" configurations. As most of these "fixes" were put in place due to a lack of ability to modify the existing system, they can now be fixed properly with the completion of the upgrade.

Linac alarms are now possible. The first critical need is alarms that indicate that "off" commands were successful. As we have seen during commissioning, failures of relays and other hardware between the PLC system and the controlled devices reduce the reliability of the overall system. Wiring and intervening devices should be simplified and corrected as one of the first upgrades. Other planned hardware upgrades include the Linac energy upgrade, the klystron focusing power supply replacement project, and water cooling upgrade project.

Software upgrades that are planned are automated pulse optimization, tuning, and operations procedures such as on, off, and standby modes. Enhanced logging of Linac parameters and waveforms are also planned.

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