DEVELOPMENT OF ULTRA-FAST SILICON SWITCHES FOR ACTIVE X-BAND HIGH POWER RF COMPRESSION SYSTEMS

Jiquan Guo*, Sami G. Tantawi, SLAC, Menlo Park, CA 94025

Abstract

In this paper, we present the recent results of our research on the high power ultra-fast silicon RF switches. This switch is composed of a group of PIN diodes on a high purity SOI (silicon on oxide) wafer. The wafer is inserted into a cylindrical waveguide under TE01 mode, performing switching by injecting carriers into the bulk silicon. Our current design use a CMOS compatible process and the device was fabricated at SNF(Stanford Nanofabrication Facility). This design is able to achieve sub-100ns switching time, while the switching speed can be improved further with 3-D device structure and faster circuit. Power handling capacity of the switch is at the level of 10MW. The switch was designed for active X-band RF pulse compression systems - especially for NLC, but it is also possible to be modified for other applications and other frequencies such as L-band.

INTRODUCTION

For years, lack of a fast Ultra-high power RF switch has kept a lot of great application ideas unrealistic. Among them is the active RF pulse compression system.

RF pulse compression systems are commonly employed to match the longer pulses from the RF sources with comparatively lower power to the loads which require shorter but higher power pulses. Such loads include, but not limit to particle accelerator structures and RF undulators. Since the development of SLED (SLAC Energy Doubler) [1], several pulse compression schemes have been studied. Active pulse compression systems using high power RF switches have attracted research interest in recent years. Theoretical studies [2] have shown that high efficiency and small system size can be achieved simultaneously in such active pulse compression systems.

Tamura has demonstrated a semiconductor PIN diode switch capable to handle 12MW RF power [3]. The switch was implemented with a PIN diode array active window. The switch is operated at the TE01 mode in circular waveguide. This mode has no radial electric field, which gives the possibility to leave a full gap in the waveguide for the active window and vacuum sealing etc without leaking RF. The PIN diodes are fabricated on a 4 inch high purity and high resistivity silicon wafer, with P and N doping lines on different sides of the wafer. During the operation, a forward bias is applied on the diodes first, injecting carriers into the silicon wafer to make it reflective to RF; then high voltage reverse bias is applied to remove those carriers and switch the wafer transparent to microwave. But the switching speed when reverse bias is applied is very slow, in the order of 100 microseconds. We analyzed the reason of the enormous long switch time for Tamura's switch. Our simulation have shown that removing carriers with reverse bias in such PIN diodes is not preferred for fast switching. When reverse bias is applied, electrons and holes move in opposite direction, strong space charge distribution cancels the reverse bias and slows down the drift speed of carriers. If higher reverse bias is applied, impact ionization will generate more carriers, making the switch speed even slower.

In the rest of this paper, we will discuss our recent research results on ultra-fast high power RF switches. The TE01 mode in circular waveguide is kept as working mode, 4 inch silicon wafers are used. The major efforts of our research are focused on the improvement of switching speed and insertion loss. Our current design is targeted for sub-100 nanosecond switching time at X-Band when forward bias is applied. Several approaches including planar structure with bulk silicon wafers, planar structure with silicon on insulator (SOI) wafers and 3-D structure have been studied. Planar structures with both bulk and SOI wafers have been fabricated and tested with low power. Other possible applications will be discussed.

DEVICE DESIGN AND FABRICATION PROCESS

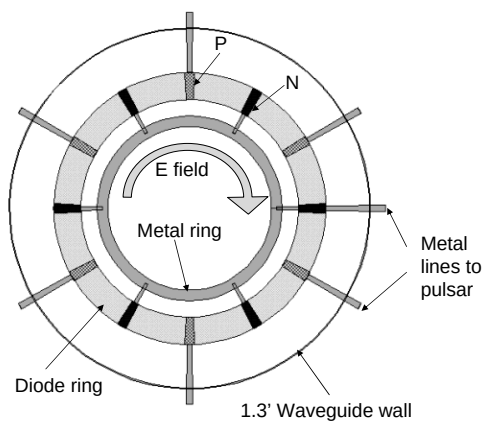

Figure 1: Schematic layout of the active window, top view

The schematic layout of the switch window is shown in Fig. 1. The window is inserted into the gap between two 1.3 inch waveguides. The P/N doping region and metal lines are radial, so they won't cut E-field under TE01 mode. The PIN diodes form a narrow ring, where the E-field is the highest inside the waveguide and the conductive silicon will reflect microwave most efficiently. There is a narrow

* jqguo@slac.stanford.edu

metal ring inside the diode ring, which has two functions: providing bias for N doped lines when metal connection from outside of the diode ring is impossible; matching the whole wafer to minimize reflection when diodes are off, helping reflection when diodes are on. The silicon inside the metal ring can be cut to reduce the loss further. The 1.3 inch diameter of the waveguide is close to cut off for our working frequency 11.424GHz, it is chosen in favor of switch speed, but will compromise power handling capacity and RF loss. Floatzone silicon wafers with 500μm thickness are used to build the switch, although thinner wafer may reduce losses further.

The structure is simulated with HFSS. When diodes are off, the window has 3% loss and 97% transmission, compared to less than 40% transmission without the metal ring. When diodes are on, assuming a carrier layer with 50μm thickness is formed under the wafer surface, transmission is less than 1%; the loss will be 10% if carrier density is 5×10^{16}/cm^3 and 3% if carrier density is 5×10^{17}/cm^3.

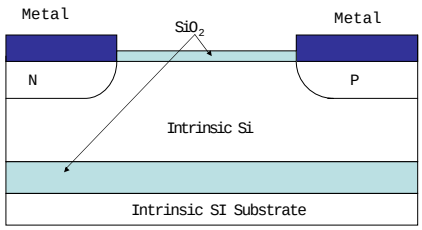

Figure 2: Structure of the Planar SOI PIN Diode

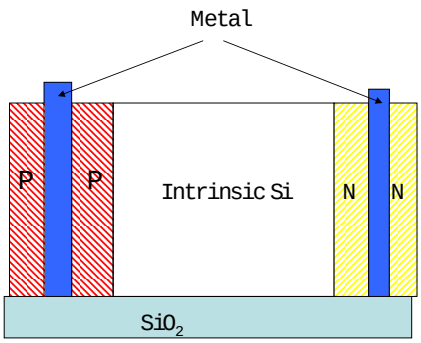

Figure 3: Structure of the 3D SOI PIN Diode

At the diode level, we have chosen planar structures instead of Tamura's double side structure. This structure is compatible with the widely used silicon CMOS process, which is available at Stanford Nanofabrication Facility (SNF). The P/N doping were completed with ion implantation and followed by a short anneal. Fig. 2 shows the structure of planar SOI PIN diode. Bulk silicon wafer structure is similar, without the buried SiO_2 layer. Devices based on both SOI and bulk wafers are fabricated. The length of the diodes (distance between P and N doping region) between 50 and 100μm, optimized for switching speed under certain available current pulse. For SOI structure, the device layer thickness is 50μm.

The fabrication process of the diodes are simulated with Tsuprem4, then the electrical property of the diodes are simulated with MEDICI, using the results from Tsuprem4. Simulation results show that, for devices with 60μm length powered by a 1KV pulsar with 1Ohm internal resistance and 30ns rise time, a 50μm carrier layer with carrier density averaged at 1×10^{16}/cm^3 can be formed in about 100ns, and reach 5×10^{16}/cm^3 in 200ns.

Planar structure devices with SOI and bulk silicon wafer are both fabricated by the author at SNF. Fig. 4 shows one of the fabricated switch.

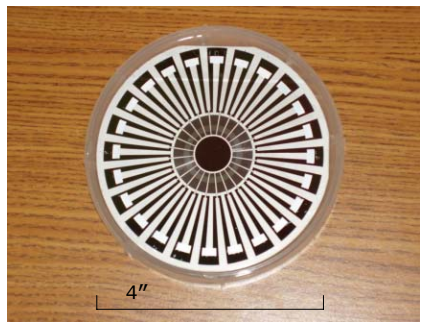

Figure 4: Fabricated active window

To enhance the switching speed further, the 3D structure shown in Fig. 3 is desirable. This 3D structure can inject carriers more uniformly into the intrinsic silicon, making the switch much faster. Our simulation shows that with same power supply, 10^{16}/cm^3 carrier density can be achieved in less than 50ns (20ns more than power supply rise time), and 5×10^{16}/cm^3 in about 70ns. However, the fabrication of this device is quite difficult compared to planar devices. A deep trench in the silicon needs to be etched for doping, then the trench needs to be filled with metal, which has not been successfully performed yet.

LOW POWER TEST SETUP AND RESULTS

Two switch setups were used in the low power test. One is the one pass setup, with the active window assembly connected with wrap-round mode converters at both end. The mode converters convert from WR90 into TE01 mode for 1.5inch circular waveguide. The test window assembly includes tapers to match from 1.5 inch to 1.3 inch circular waveguide. This directly characterize the active window. The other setup is the switch module shown in Fig. 5. Port 1 and 4 of a magic T is connected to input and output. Port 2 of the magic T is connected to a movable short, which can tune S matrix when active window is reflective; port 3 is connected to active window, with a movable short on the back to tune when active window is transparent.

Cold Test

Cold test of the switch is performed to characterize the switches at off state. Network analyzer is used in the

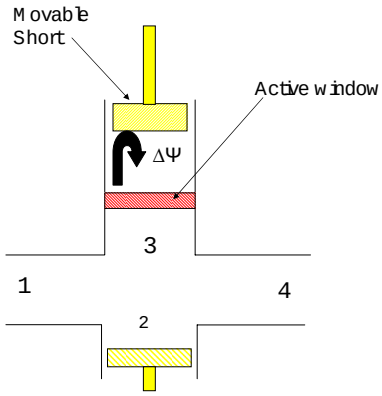

Figure 5: Skematic view of the switch module

test. For bulk silicon device batch 1, we have S_{11}=0.4 and 10% loss when a whole is cut in the center. Compared to S_{12}=0.75 for devices without the metal ring in the center, it's a good improvement. But it's still off from our simulation. One reason of the discrepancy is that the switch assembly was not well matched. For bulk device batch 2, we reduced the anneal time, so the loss is reduced to 6%. Considering the loss in the waveguide and mode converters, it's inline with our simulation.

The blank SOI wafers we obtained from vendor has higher impurity than required, resulting 30% loss in the SOI devices.

Low Power Test

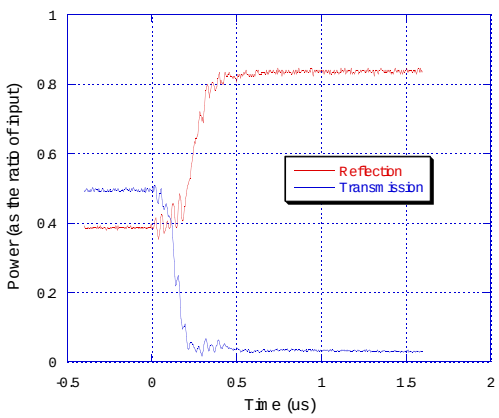

Figure 6: Time response of the Bulk Silicon Switch

Low power test is performed both with one pass setup and the module setup. Pulsed power meter was used to measure the input and the transmitted/relected power through directional couplers. The switch is powered by a home made circuit, using one IXYS EVDD408 evaluation board driving 2 IRGPS60B120KD IGBTs (or EVDD414 driving 4 IGBTs). 900V/1.2kA with about 40ns rise time was achieved by 4 IGBTs driven by 2 EVDD408.

Fig. 5 shows the time response of bulk silicon switch with one pass setup. Switch time is about 300ns, with 15% loss. about $1mu$s switch time and 30% loss was observed for the switch module setup.

DISCUSSION

Our research has demonstrated 300ns switch time for a bulk silicon X-Band RF switch. Although we have simulated 1-200ns switch time for SOI planar switch, our fabrication of the SOI switches was not successful due to the quality of the blank SOI wafers does not meet our requirement. For sub-100ns switch time, 3-D structure with deep trenches is a possible solution, although the metalization of the trenches needs to be studied. The power handling capacity of these switches has not been tested yet.

Another potential application of this semiconductor switch is on pulsed superconducting RF accelerator structures, like in the International Linear Collider (ILC). Although those structures do not need pulse compression systems, extracting the stored RF energy out of the structures between pulses is mandatory to reduce the wall loss inside the structure. Since the superconductor RF structures typically work at liquid Helium temperature, the cryogenic system needs about 600 Joule power to remove 1 Joule heat generated by the wall loss [4].

The semiconductor switch is an ideal choice for that extraction function. Since most of those superconducting structures are working at lower frequency like L-Band, the loss in the wafer is much less. The required switch time is not as critical as in the pulse compression systems. The size of the devices will be larger, so the power handling capacity will be higher. However, the size of devices also limits the lowest frequency. In case that the 4 inch silicon wafers are used, the lowest frequency can be handled is about 1.2GHz, with alumina filled in the circular waveguide.

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