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DESIGN CONSIDERATIONS FOR THE STABILITY IMPROVEMENT OF KLYSTRON-MODULATOR FOR PAL XFEL*

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Abstract

The PAL (Pohang Accelerator Laboratory) 2.5-GeV linac is planed to be converted to a SASE-XFEL facility (PAL XFEL) that supplies coherent X-rays down to 0.3-nm wavelength. The PAL XEL requires a new 1.2-GeV linac that will be combined to the existing linac to increase a beam energy upto 3.7-GeV. This XFEL linac should supply highly bright beams with emittance of 1.2 mm-mrad, a peak current of 3.5 kA, and a low energy spread of 0.03%. The RF stability of 0.02% is required for both RF phase and amplitude to get stable SASE output. This stability is mainly determined by a low level RF drive system and klystron-modulators. The stability level of the modulator has to be improved 10 times better to meet the pulse stability of 0.02%. The regulation methods such as traditional de-Q'ing and precision inverter charging technology are reviewed to find out suitable upgrade shceme of the modulators. Design considerations for the stability improvement of klystron-modulators for PAL XFEL are presented.

INTRODUCTION

PAL XFEL is a 4th generation light source that is a coherent X-ray free electron laser (FEL) by utilizing an existing 2.5-GeV linac [1], [2]. This source is based on the principle of Self Amplified Spontaneous Emission (SASE), single-pass high-gain FEL. The SASE is only possible by low emittance and extremely dense electron bunches moving in an undulator magnetic field. A short-period undulator will give a compact FEL machine for a short-wave radiation. An in-vacuum undulator is essential to produce coherent X-ray radiation at wavelengths down to 0.3 nm with a beam energy of less than 4-GeV.

By adding an RF photo-cathode gun, two bunch compressors, and a 1.2-GeV S-band injector linac to the existing 2.5-GeV PLS linac, the PLS linac can be converted to a SASE XFEL facility which supplies coherent X-ray down to 0.3-nm wavelength. The linac should supply highly bright beams with parameters summarized in Table 1.

Table 1: Beam parameters of PAL XFEL

Maximum beam energy	3.7 GeV
Normalized emittance	1.2 µm
FWHM bunch length	0.23 ps
RMS energy spread	< 1 MeV
Maximum bunch charge	< 1.0 nC
Peak current	3.5 kA
Repetition rate	60 Hz

The RF stability is a key issue to get stable SASE output. A low level RF drive system and klystron-modulators hasve to be upgraded to provide stable operating conditions. The stability level of the modulator has to be improved 10 times better to meet the strict pulse stability. This paper shows the suitable upgrade shceme of the modulators and design considerations for the stability improvement of klystron-modulators for PAL XFEL.

STABILITY REQUIREMENT

In order to realize a stable beam at the end of linac, the linac system should meet a condition,

$$\sum_{i=1}^{n}\left(P_{tolerance}/P_{sensitivity}\right)^{2} \ \langle\ 1,$$

where $P_{tolerance}$ is a technically achievable tolerance partly affecting the system performance and $P_{sensitivity}$ is a maximum allowable tolerance assuming no any other error source. The analysis of the jitter sensitivity of PAL XFEL is base on the threshold of FEL performance: peak-to-peak change in SASE wavelength less than 0.5%, peak-to-peak change in saturation length less than 10%, peak-to-peak change in saturation power less than 40%, and peak-to-peak change in bunch arrival time less than 50 fs.

The linac system is characterized by two groups, X-linac and K-linac as shown in Figure 1. The X-linac is a new 1.2-GeV linac and the K-linac is the existing 2.5-GeV linac.

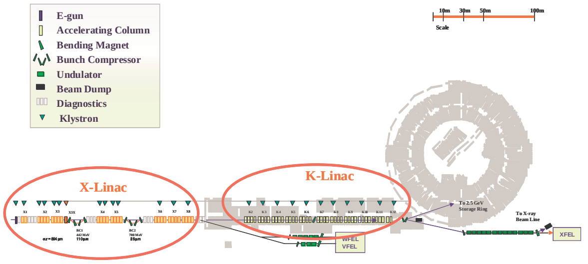

Figure 1: XFEL linac configuration.

The previous jitter analysis shows that the RF gradient stability tolerance of the X-linac is almost 10 times tighter than the K-linac as shown in Table 2 [3].

Table 2: RF jitter tolerance of PAL XFEL

Parameters	Sensitivity	Tolerance
X1 Gradient	-0.06%	0.02%
X2 gradient	-0.11%	0.02%
X3X gradient	+0.29%	0.02%
K2 gradient	+1.7%	0.1%

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The tight jitter tolerance can be relaxed by operating more klystrons in one accelerating section. One klystron will be dedicated to two S-band accelerating columns from X1 to X5 sections to relax tight jitter tolerance. Since each two accelerating columns will be operated by their own klystrons under the same RF conditions, all units in the X-linac have the same jitter sensitivity. Since jitter tolerance is loose at the downstream of BC2, one klystron will be dedicated to four S-band accelerating columns from K2 to K12 sections. Also tight jitter tolerance can be looser by operating S-band accelerating columns around bunch compressors with a low gradient of about 15 MV/m.

K-LINAC MODULATORS

The existing modulators in K-linac uses traditional resonant charging scheme. The charging voltage regulation of K-linac is done by a de-Q'ing circuit. PAL modulators have a simple de-Q'ing controller and test results show the stability of 0.2%.

The status of existing de-Q'ing technology is as follows. Modulators at SPring-8 injector linac regulate the charging voltage with stability of 0.03% by using an IVR and de-Q'ing % optimization. Modulators at ATF in KEK regulate the charging voltage with 0.01% stability by using a feed-forward de-Q'ing. SLC modulator provides 0.03% stability by waveform compensating de-Q'ing.

Therefore the existing system can be easily improved to match the stability requirement by adopting a standard de-Q'ing method with modern digital control circuit adopted by ATF modulators.

X-LINAC MODULATORS

Figure 2 shows the basic circuits and their charging waveforms for a voltage source (resonant charging) and current source (inverter charging). An inverter technology provides high reliability, and command charging function. It is inherently short-circuit safe. In addition, it is naturally compact. There are other attractive features: expandability, easy maintenance, and flexible control interface. It is not necessary De-Q'ing system and bulky EOLC thyrite. These features are well matched to the requirements of X-linac modulators. The tight tolerance and dynamic control of a charging level can be reasonably achievable with an inverter power supply.

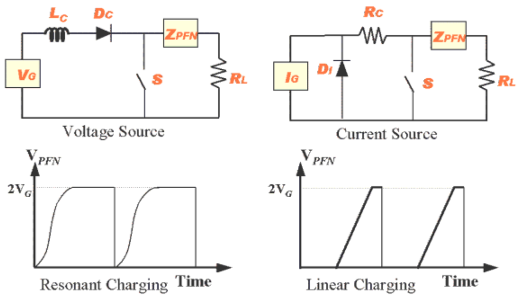

Figure 2: Basic circuits and charging waveforms of a voltage source and a current source power supply.

INVERTER TOPOLOGY

A typical series-resonant inverter (SRI) shown in Figure 3 is simplest and oldest topology that uses on/off control of constant switching frequency so that the switching frequency, f_{sw} is less than a resonant frequency, f_r. The minimum burst size of charge bucket, Q is I_o / f_r and corresponding minimum voltage step, V is Q/C.

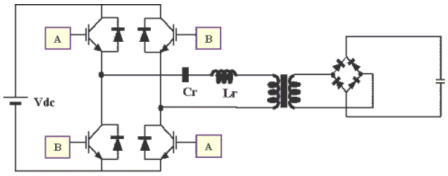

Figure 3: Series resonant inverter.

A PWM (pulse width modulation) inverter uses same circuit as series resonant inverter. It can rapidly charge a load capacitor by constant switching mode up to specified charging lever then the rest charging is done by fine regulation using a pulse width modulation mode. A charge bucket can be is reduced to 10% of the regular size. The repeatability can be improved 2-3 times easily.

A parallel resonant inverter (PRI) as shown in Figure 4 has a parallel capacitor on the secondary side of the transformer. It can change the switching frequency. Rapid charging at resonant frequency is commanded first then a current is reduced by increasing a switching frequency above f_r. The stored energy must be discharged between each pulse.

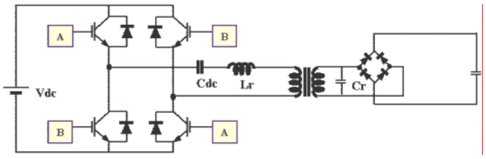

Figure 4: Parallel resonant inverter.

A phase-shifting resonant inverter (PSRI) as shown in Figure 5 has two independent inverter circuits. It operates a constant switching frequency with an independent phase control of each inverter. A rapid charging is done at synchronized or in phase switching then a current reduction is done by phase shift between the switching cycles.

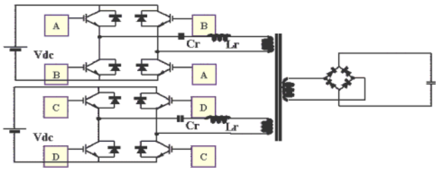

Figure 5: Phase shifting resonant inverter.

The most simple and straight way is to use several inverters in parallel. Rapid charging is done by high power units and a fine regulation is done by a designated small power unit. Repeatability is depends on the small charging unit.

The present status of the pulse-to-pulse repeatability of available inverters is summarized in Table 3.

Table 3. Regulation status of charging inverters

Method	Rating	Maker	Regulation
SRI	8 kJ/sec	GA	0.5%
PWM	8 kJ/sec	GA	< 0.25%
PSRI	7 kJ/sec	Lamda-EMI	0.2%
SRI	9 kJ/sec	Lamda-EMI	4% @ 1 kHz
SRI	37.5 kJ/sec	Lamda-EMI	1% @ 100 Hz
SRI	37.5 kJ/sec	Toshiba	0.035%

The thermal drift of 0.5% in the feedback and reference voltage components is possible for all power supplies. The switching frequency of an inverter is 50 kHz for GA and 40 kHz for Lamda-EMI. The electric conversion efficiency is about 90% for GA and about 85% at full load for Lamda-EMI. In general, the power factor is larger than 0.85 at full load. The long-term stability is 0.1% for 8 hours after 1.5-hour warm-up and 0.2% per hour after 1-hour warm-up for Lamda-EMI. The nominal accuracy is about ± 0.5%. The stored energy is limited less than 0.3 Joules for Lamda-EMI. The high voltage resistor has the temperature coefficient of 100 PPM/ºC for Lamda-EMI.

PARALLEL INVERTER APPLICATION

The cost effective and simple configuration of the inverter topology for X-linac modulator is parallel operation with matched fine charging unit. The coarse charging and fine charging is arranged to get the regulation with optimum power sharing. Figure 6 shows the charging schedule with parallel operation of inverters.

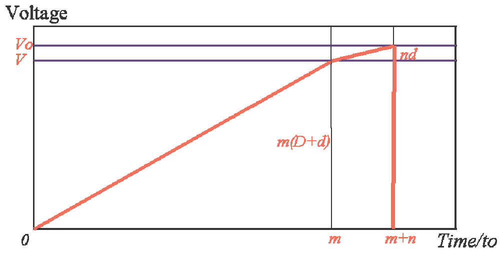

Figure 6: Charging schedule with parallel operation.

Total charging time T_c and charging voltage V_o are given by

$$(m+n)\, t_o = T_c\, ,\ m\, (D + d) + n\, d = V_o\, ,$$
$$n\, d = V_o - V = j\, D\, ,$$
$$m+n = a,\ m^2 - a\, m + (a + b)\, j = 0\, ,$$

where inverter switching time $t_o = 1/\, f_r$, T_c is total charging time, m is total switching number of coarse charging, n is total switching number of fine charging, $a = T_c\, /\, t_o$, fine charging step $d = I_f\, t_o\, /\, C$, coarse charging step $D = (I_c + I_f)\, t_o\, /\, C$, C is a load capacitance, I_f is charging current of a fine inverter, I_c is charging current of a coarse inverter.

Typical parameters for PAL XFEL modulator are PRR = 60 Hz, f_r = 30 kHz, V_o =50 kV, C =1.2 uF, b = 10,000. Then T_c = 16.7 [msec], t_o = 33.3 usec, a = 500, P_{av} = 90 kJ/sec. Figure 7 shows the calculated result of charging power and charging current sharing. The main inverter charging current, I_c is 3.73 A, and a fine charging current, I_f is 0.18 A. The main charging power, P_c is 93.23 kJ/sec, and fine charging power, P_f is 4.5 kJ/sec.

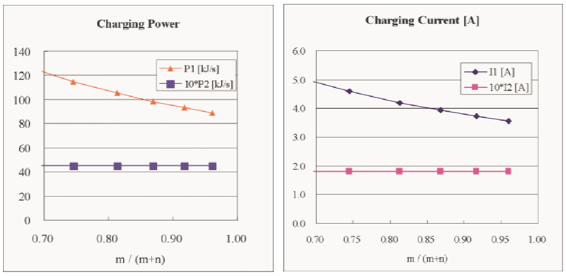

Figure 7: Charging power and charging current sharing.

A voltage feedback circuit must have a stable high voltage monitor independent from a power supply. Temperature coefficient of resistor and capacitors are typically 10-100 PPM/ºC and 0-4700 PPM/ºC. Therefore temperature coefficients matching between resistors and capacitors are also important. Achievable stability is expected to be about 1-5 PPM/ºC. Stable temperature control is essential for stable feedback.

SUMMARY

The jitter tolerance of 1.2-GeV FEL linac is tight. Especially jitter tolerance of a photo-injector is so tight. Jitter tolerance of existing 2.5-GeV linac is rather easily achievable. De-Q'ing is cost effective way for existing 2.5–GeV linac. The best stability of an available inverter is about 1000 PPM. Many possible circuit topologies can be combined for better regulation. Minimum charge bucket is essential parameter. We need temperature stabilization and separate stable voltage monitoring. The stability of 100 PPM is easily achievable. The stability of 10 PPM is technically achievable.

ACKNOWLEDGMENTS

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