REAL-TIME BEAM LOSS MONITOR DISPLAY USING FPGA TECHNOLOGY

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Abstract

This paper outlines the design of a Real-time Beam Loss Monitor Display for the ISIS pulsed neutron source based at the Rutherford Appleton Laboratory (Oxon, UK). Synchrotron beam loss is monitored using 39 argon filled ionisation chambers positioned around the synchrotron, the levels of which are sampled four times in each cycle. Four histograms relating to synchrotron beam loss are generated and displayed within each machine cycle (50Hz). Attributes of the new system include setting limits for individual monitors; displaying excursions through limits and freezing the display field on demand. The design is based around a reconfigurable Field Programmable Gate Array (FPGA), interfacing to a TFT monitor via the VGA standard. Results gained using simulated monitor signals have proven the system.

INTRODUCTION

ISIS is currently the world's most intense pulsed spallation neutron source, located at the Rutherford Appleton Laboratory, Chilton, Didcot UK. The facility operates for ~ 200 days per year supporting a large international community researching physics, chemistry, materials science, geology, engineering and biology.

The facility consists of an H- ion source, 665 KeV RFQ, 70 MeV Linac, 800 MeV Synchrotron and associated beam transfer lines. Successful operation and maintenance of the facility requires high levels of beam loss control. The beam transfer efficiency in each accelerator is monitored using beam intensity monitors and beam loss monitors.

The beam loss monitors (BLM) used on ISIS are of the Brookhaven type [1], argon gas filled ionisation chambers which are sensitive to thermal neutrons induced by beam loss events. There are approximately 80 BLM's distributed around the facility, 39 of which measure loss in the synchrotron. As part of an ongoing obsolescence programme the data acquisition (DAQ) and signal visualisation for the synchrotron monitors are being upgraded. This paper reports on the upgrade.

EXISTING BLM DISPLAY SYSTEM

A block diagram of the current BLM diagnostic system is shown in Figure 1. The highlighted area indicates the part of the system being replaced. The Graphics Micro-Computer (GMC) is replaced by a graphics processor, the fast raster scan VDU is to be replaced by a modern TFT monitor.

The GMC acquires 39 sample and held BLM signals over four user defined integration periods. The start of each integration period is referenced to the ISIS timing bus, providing beam loss integration at distinct periods in the machine cycle.

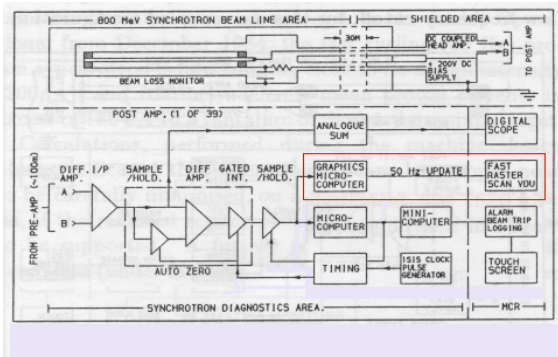

Figure 1: 800 MeV BLM system schematic.

A histogram is then generated for each period and displayed on a fast raster scan VDU. This VDU is located in the ISIS Main Control Room. The current system operates at 25 Hz, half the accelerator operating frequency. The integration periods are usually specified to cover Synchrotron Injection, Trapping, Acceleration and Extraction. An impression of the display is shown in Figure 2. Each bar is a BLM signal. Red bars show beam loss has exceeded a tolerance limit.

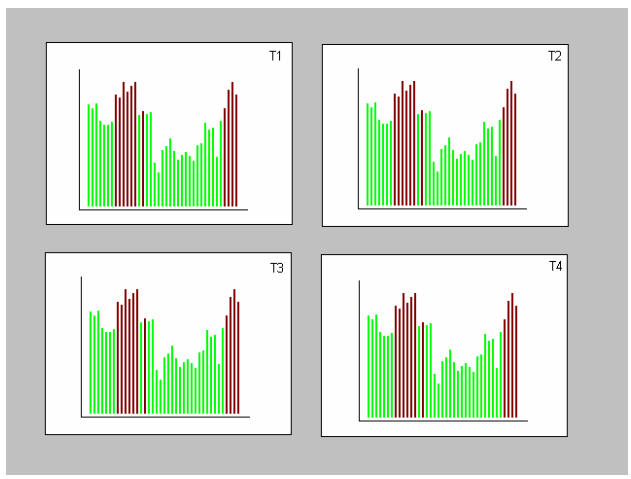

Figure 2: Beam loss monitor display.

NEW BLM DISPLAY SYSTEM

Design Specification

The new BLM system was specified to display data in the same form as the existing system, including two new functions. Firstly display data in real time, at the machine

frequency of 50Hz. Secondly freeze the display for a programmable period. The specification for the new design is as follows.

- Sample data from 39 BLM's at four programmable sampling points every 50 Hz.
- User defined tolerance levels for each BLM.
- Graphically indicate an excursion through a tolerance level.
- Display BLM data in histogram form, at 50 Hz.
- Freeze display on demand.

Field Programmable Gate Arrays

The new graphics processor is based around an FPGA. The processing architecture of the FPGA is designed through Hardware Description Languages (HDL). Hence the integrated circuit (IC) is application specific enabling high speed designs incorporating wide data busses and parallel operations. Due to the amount of data acquisition and processing required in this design, an FPGA was an ideal solution.

The BLM display utilises the Lattice Semiconductor expanded programmable gate array (XPGA). The XPGA is an unconventional FPGA as it incorporates E^2PROM and SRAM memories when programming. This makes the XPGA appear non-volatile.

Data Acquisition

A bank of 5, 8-channel, 8 bit serial Analogue to Digital Converter (ADC) are used to acquire the 39 sample and held BLM signals. Each is sampled at a frequency of 25MHz; relating to a conversion rate of 1.39MHz after serial decoding. Therefore the time to acquire all BLM signals is given by:

$$T_{conv} = \frac{8}{1.39x10^{6}} = 5.75\mu S \qquad (1)$$

Hence the throughput rate for data acquisition is:

$$S = \frac{39x8}{5.75x10^{-6}} = 54.26Mbps \qquad (2)$$

Aquired data is registered into an 8x8 bit array. Control, decoding and registering of each ADC stream is executed in parallel by the FPGA.

Video Processing

Figure 3 highlights the main VHDL components instantiated into the FPGA. Video processing is required to interpret acquired data, manipulating this data into pixel position and RGB colour information, ensuring that histograms are displayed on the monitor. Video memory is required to store the RGB data for each pixel. The Video Graphics Array (VGA) standard supports a field resolution of 640x480 pixels with 4 bit colour (16 colours). Employing a bitmap scheme would require the following video memory allocation:

$$M_{VGA} = \frac{(640 \times 480)(4 \times 3)}{8} = 460.8kBytes \qquad (3)$$

However the XPGA only has 14kBytes of embedded memory. A novel scheme was engineered to reduce this overhead.

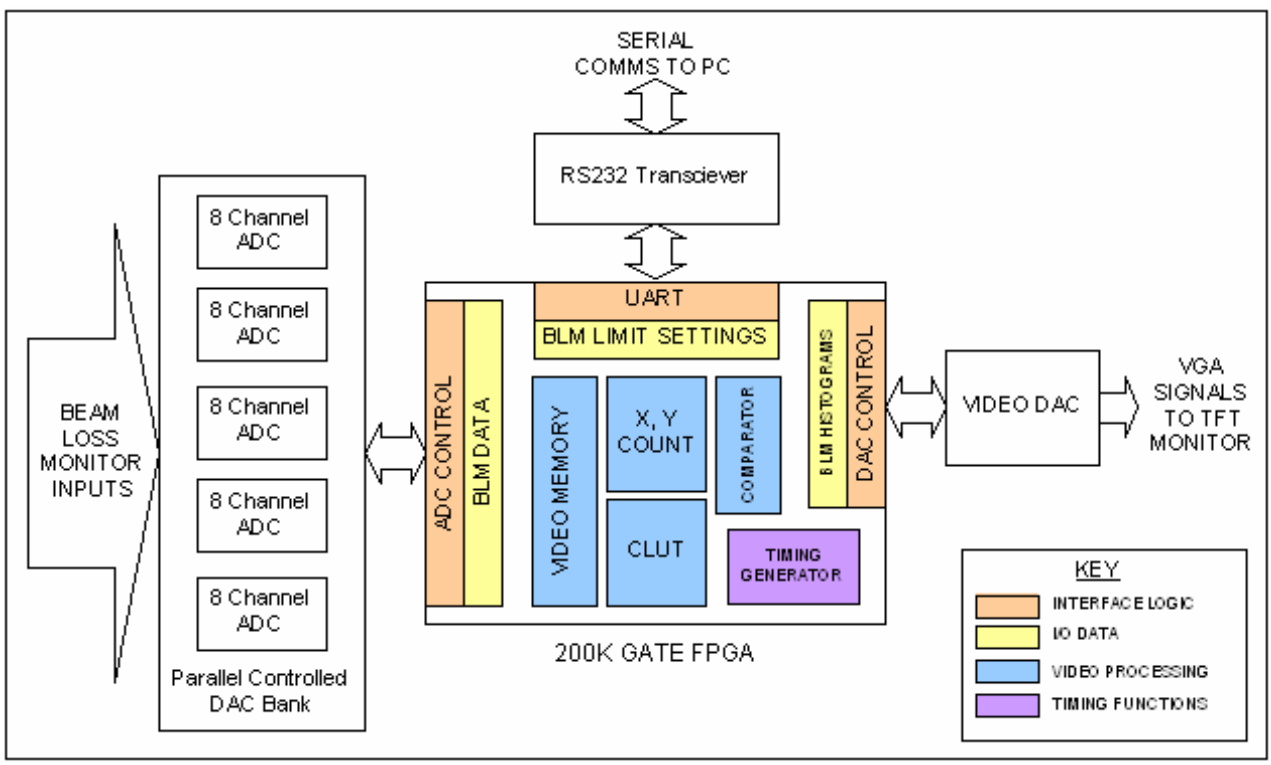

Figure 3: Block diagram of BLM display system.

Video Memory Reduction

The majority of the BLM display frame holds no information. Therefore the frame can be split into two fields, background and histogram.

The background field contains three colours. Hence two bits of colour information are needed to represent the entire background. Co-ordinates for the current pixel position are generated using (X,Y) counters. The counters are clocked by video synchronisation pulses and pixel ticks. These co-ordinates are used to map the colour changes throughout the background field and indicate sub-field areas. Each sub-field relates to a histogram area, the histogram displays 39 bars each with an area of 2x128 pixels. Therefore 39(2x128**)** pixels would be required for an entire histogram. A scheme was devised using the BLM histogram array to generate the histogram bars. The counters, X_{sf} and Y_{sf}, produce co-ordinates normalised to the sub-field area. As the active pixel raster moves through the sub-field, the X_{sf} coordinate addresses both BLM histogram array and BLM limit array. A comparison is made; the outcome of which holds the pixel colour information. The histogram bar is only one of two colours; indicating BLM signal excursion through a limit. Therefore only 1 bit of colour information is needed for the entire data set. Hence the required video memory has been reduced to;

$$M_{Total} = M_{CLUT} + \left(M_{BLM} \times 4\right) \tag{4}$$

$$M_{Total} = \frac{\left(8 \times 5\right) + \left(8 \times \left(39 \times 4\right)\right)}{8} = 161 Bytes \tag{5}$$

This is a significant memory saving and can be easily accommodated in the XPGA memory.

Freeze Frame

Design specification requires the frame to be frozen on demand. This allows a significant beam loss event to be viewed by a user for a programmable period. This function was implemented by not loading new BLM data into the histogram memory when an external signal is asserted. The pulse width of this signal is controlled externally and relates to the freeze frame period.

Interfacing

Figure 3 indicates that, disregarding data acquisition, there are two interfaces between the graphics processor and the outside world; via RS232 for programming BLM limits and through a video Digital Analogue Converter (DAC) displaying data on the monitor.

BLM limits are set by a local computer. A simple Universal Asynchronous Receiver Transmitter (UART), implemented in the FPGA, provides transmission rates up to 9600 baud with odd or even parity checking.

A colour look up table is used to decode 1 or 2 bit colour information into 8 bit RGB data, interfacing to the video DAC.

TESTING

Simulation of Very High Speed Integrated Circuit Hardware Description Language (VHDL) components produced some good results. However simulation results for video components were hard to verify. Therefore VHDL components relating to frame generation were written during the testing phase. Results could be easily verified on the test monitor.

Test Set-up

Testing apparatus consisted of a signal generator and a TFT monitor. Live BLM signals were not available during bench testing. A test box was designed to propagate the signal generator output through 39 paths; allowing variable attenuation.

Results

Testing proved the system. Generation of stable real time histogram data was achieved. Limits can be set and indicated. The frame can be frozen on demand. Commissioning is planned to take place in the coming months. There are plans for the system to be used throughout the ISIS facility, monitoring beam loss in the 70 MeV Linac, Extracted Proton Beamline (EPB), and the future second EPB for Target Station 2.

FUTURE RECOMMENDATIONS

Modifications need to be made to the UART enabling a PC to read the histogram arrays. This will allow beam loss data logging and offline analysis.

Limit settings for each BLM signal should be displayed. Beam loss beyond a threshold setting should be indicated by a portion of the bar changing colour, not the entire bar.

ACKNOWLEDGEMENTS

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REFERENCES

[1] M.A. Clarke-Gayther, A.I. Borden and G.M. Allen, “Global Beam Loss Monitoring Using Long Ionisation Chambers at ISIS”, EPAC’94, London, July 1994, p. 1634.