JEFFERSON LAB'S TRIM CARD II*

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Abstract

Jefferson Lab's Continuous Electron Beam Accelerator Facility (CEBAF) uses Trim Card I power supplies to drive approximately 1900 correction magnets. These trim cards have had a long and illustrious service record. However, some of the employed technology is now obsolete, making it difficult to maintain the system and retain adequate spares. The Trim Card II is being developed to act as a transparent replacement for its aging predecessor. A modular approach has been taken in its development to facilitate the substitution of sections for future improvements and maintenance. The resulting design has been divided into a motherboard and 7 daughter cards which has also allowed for parallel development. The Trim Card II utilizes modern technologies such as a Field Programmable Gate Array (FPGA) and a microprocessor to embed trim card controls and diagnostics. These reprogrammable devices also provide the versatility to incorporate future requirements.

INTRODUCTION

Jefferson Lab uses 1 to 12 A series pass regulator power supplies, known as Trim Card I, to control approximately 1900 X-Y dipole steering magnets, focusing quadrapole magnets, and solenoids throughout CEBAF. This programmable, 200 W, bipolar, power supply has performed reliably for over 12 years. However, the rapid evolution of electronic components has resulted in its obsolescence and the need for piggyback adapter boards to replace discontinued technologies. New additions to the CEBAF beam line have been common throughout its evolution. These devices often require different output voltages, output currents, and programming characteristics such as specific current-ramp profiles. The Trim Card I is limited in its capability to incorporate the needs of these new devices. The card is also lacking diagnostic and self-check features that would facilitate quick diagnosis and shorter repair times. A new generation plug-compatible supply is being developed to replace the Trim Card I. The redesigned Trim Card II addresses the issues of obsolescence, flexibility, and diagnostics by taking a modular design approach and using up-to-date components [2, 3].

Design Approach

The original Trim Card I was realized as a single plug-in circuit board, approximately 9" H x 20" D. Thirty two trim cards are housed in card-cages within a single rack. With the exception of sharing common bulk power supplies, each trim card is a complete stand-alone, programmable, precision, constant-current power supply including a microprocessor, Digital to Analog Converter (DAC), regulator section, power amplifier, two Analog to Digital Converters (ADC), and supporting circuitry. External programming commands and data read backs are exchanged with the Experimental Physics and Industrial Control System (EPICS) via a RS-485 data link, shared by all 32 cards in the rack [1].

Flexibility and freedom from obsolescence prompted a highly modular approach to the design of the new Trim Card II. Most circuit functions were realized as daughterboard modules. Only the Power Amplifier section, with its large heat-sink, is a permanent part of the Motherboard. The remaining circuits components where divided into the Analog Block, Drive Module, Analog Monitor, CPU Module, RS-485 Module, Display Module, and Temperature Sensor. Figure 1 illustrates how these components are interconnected.

The mother/daughterboard concept has several advantages. The individual modules are designed, produced, tested, and stocked individually and in parallel. Future modifications may be incorporated into one modular board without requiring scrapping or rework of the entire trim card. Repairs may be accomplished quickly by replacing an individual daughter board. Bench repair of a daughter board is facilitated by dedicated test sets which are simpler, smaller, and safer than the test fixture for an entire trim card. The disadvantages of the daughter board concept include the extra overhead of designing and maintaining multiple modules as well as the increased risk of mating and corrosion issues due to multiple connectors.

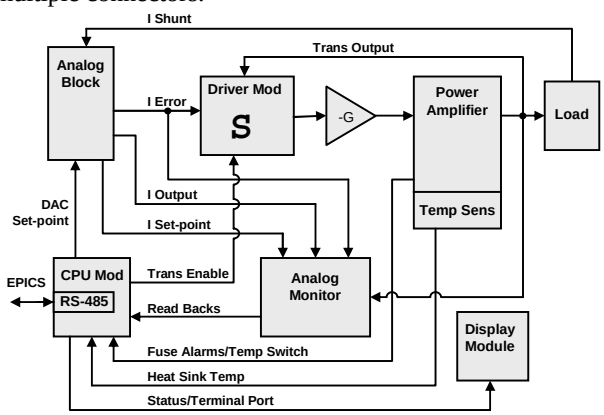

Figure 1: Trim Card II block diagram.

MOTHERBOARD

The Trim II Motherboard is designed to be physically and electrically compatible with the existing card cage

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and controls. The main objectives of the Motherboard are to interconnect all the daughter cards, distribute power to the daughter cards, and house the Power Amplifier section.

A 48-pin connector, mounted on the rear apron, engages a mating connector in the card cage where +/- 27V bulk power, 5V power, and RS-485 communication are derived. The incoming power is fused appropriately and distributed to the daughter cards. Three epoxy-coated copper buss bars are used to route bulk power and load output from the rear connector to the Power Amplifier section. These buss bars also provide a measure of mechanical rigidity to an otherwise flexible board. Two large transient voltage suppressor diodes insure that the incoming bulk supply rails are clamped a few volts above nominal. These diodes also provide a path to dissipate energy stored in the inductive load in the event of an abrupt change in programmed output current. A 5V DC-to-DC converter is also included to eliminate the need for an external 5V supply for digital circuits.

Power Amplifier

The Trim Card II uses a pass bank of power transistors to control output current to the magnet load. The transistors operate in the linear mode where the output current is a function of the transistor base drive. The transistors are arranged in a half H-bridge to achieve bipolar operation with current flow to the magnets supplied by PNP transistors in the positive direction and NPN transistors in the negative direction.

A common collector configuration is employed to provide maximum impedance as viewed from the load and to utilize to the maximum extent of the voltage available from the bulk supplies. This setup avoids an oscillatory condition inherent in common emitter configurations. A 1 ohm resistor is placed in the emitter circuit of each of the 6 parallel pass transistors to encourage current sharing.

The collector cases of both the PNP and NPN transistors are at the same potential which allows them to be mounted directly to the same finned heat sink without insulating wafers. This reduces the thermal impedance between the transistors and heat sink for maximum power dissipation. Conduction occurs in only one pass bank arm at a time so the locations of the PNP and NPN transistors are alternated on the heat sink to maximize its thermal efficiency. The heat sink is capable of dissipating up to 200 W and is cooled with forced air. A thermal switch removes the base current drive if the heat sink exceeds 65 degrees C. Each transistor is individually fused. Fuse status information is collected and transmitted to the CPU Module via a Serial Peripheral Interface (SPI).

ANALOG BLOCK

The Analog Block precisely regulates the load current. An internal 16-bit DAC generates the programmable current set-point reference signal and is controlled by the CPU Module via SPI. A shunt resistor is used to determine the maximum achievable current output and to provide a current output feedback signal that is proportional to load current. These two signals are compared at an op-amp summing junction to generate the current error signal. This output is applied to the Driver Board to correct the output voltage and hence, the output current. The current set-point, output, and error signals are buffered and sent to the Analog Monitor. Three bits that represent the shunt resistor value are sent to the CPU Module to indicate the maximum current output of the trim card. The hand tuned zero and scale adjustments of the DAC voltage form the basic calibration points of the trim card. The DAC and the current shunt resistor have very low temperature coefficients that eliminate the need for temperature regulation which was present in the original Trim Card I.

DRIVER MODULE

The Driver Module provides the base drive to the pass bank transistors. It uses feedback from the transistor output to transform the Power Amplifier into a voltage regulated amplifier. By placing the entire Power Amplifier within a voltage feedback loop, the transfer function of the amplifier remains constant despite any internal changes in gain. The inductive magnet load responds quickly to the internal voltage-regulated loop. This allows for the suppression of any voltage ripple originating from the bulk supply busses. The current error signal from the Analog Block's slower constant-current loop is used to compensate for changes in magnet resistance due to temperature.

The Trim Card II Class C setup suffers from a discontinuity when conduction changes from the positive to negative pass bank transistor arm as the output passes though the zero point. Although the effect is suppressed by the feedback loops, this interruption can be problematic during fast ramps or step changes. The Driver Board employs individual biasing adjustments for the transistor base current drives. This maintains some conduction in both bank arms as the output passes through zero, thus minimizing the distortion.

A set of transistor enable relays are in series with the base drives of the pass bank transistors. These relays are used to turn off the current flow to the load and are controlled externally by the CPU Module, thermal switch, and transistor enable switch. This allows the Trim Card II to be hot-swapped without damaging equipment.

ANALOG MONITOR

The Analog Monitor is an 8 channel differential ADC board used to measure various trim card signals. The front end includes a multiplexer and instrumentation amplifier with selectable gains. The channels and corresponding gains are selected by a FPGA which then instructs the 100 ksps 16-bit ADC to sample. The FPGA processes the digital ADC data and then transmits the results to the CPU Module via SPI. Onboard memory is

also available to buffer fast ADC data and may prove to be a useful diagnostic tool for future applications.

The Trim Card II signals that are monitored include the current set-point, error, and output from the Analog Block and the voltage output from the Power Amplifier. These readings are used to determine if the trim card is regulating the current correctly. The +/-27 V bulk supplies are also monitored as a health check.

A precision 5V reference and ground reference are sampled and used by the FPGA to automatically compensate for offset and gain inaccuracies. This compensation is preformed in conjunction with digitally filtering the inputs to give the most accurate result.

CPU MODULE

The CPU Module controls the trim card and communicates with the EPICS control system. A 16-bit Motorola HCS12 microcontroller writes to the Analog Block's current set-point DAC via the first SPI bus. Using 3 input pins, it also reads the Analog Block shunt resistor indicators that represent the maximum output current from the trim card. The Driver Module's transistor enable relay is driven by an output pin. The transistor enable relay, thermal switch, and transistor enable switch statuses are read back with input pins. ADC data is collected from the Analog Monitor using the second SPI bus. The first serial communications port is connected to a RS-232 transceiver and routed to the front of the Motherboard. It is configured as a terminal port and used for troubleshooting and diagnostics. The third SPI buss is shared by 3 devices including the fuse alarm indicators from the Motherboard, the Display Module, and the Temperature Senor. The second serial communications port is used to drive the RS-485 Module and thus communicate with EPICS.

Display Module

The Display Module plugs into the front of the Motherboard and is visible when the trim card is installed in a card cage. It uses 7-segment displays and LED indicators to provide status and error information. The 7-segment displays are controlled by the CPU Module via SPI and the LED indicators are driven by logic signals.

Temperature Sensor

The Temperature Sensor board incorporates a 12-bit plus sign digital temperature sensor and mounts to the heat sink. It is polled by the CPU Module via SPI buss and is used to set warning flags or shutdown the trim card if the Power Amplifier section overheats.

RS-485 Module

The Trim Card I RS-485 circuitry has failed frequently due to transients on the external communication lines. The RS-485 Module for the Trim Card II was developed as an easily-replaceable granddaughter board that plugs into the CPU Module. It functions as a RS-485 transceiver to facilitate communications between the CPU Module and EPICS.

EPICS Interface

A single board computer, running the VxWorks real time operating system, is used to control the trim cards via EPICS. A data acquisition task communicates with the trim cards using RS-485 IP-Packs. The task reads ADC and status information from each trim card at a rate of 10 Hz. New current set-points and the transistor enable commands are sent out on demand at the maximum rate of 10 Hz. The Trim Card II was designed to be compatible with the existing data acquisition task used with the Trim Card I.

Microcontroller Program

The microcontroller program consists of 2 interrupt service routines. The serial interrupt service routine is used for handling RS-485 communication between the trim card and the EPICS data acquisition task. The other interrupt service routine sets up a semaphore to execute the main loop every 50 milliseconds.

The main loop monitors the health of the trim card by checking the statuses of the transistor fuses, enable switch, enable relay, and thermal switch. It also reads in the ADC values from the Analog Monitor and Temperature Sensor to verify that they are in the appropriate windows. Error conditions result in the Analog Block DAC set-point being forced to 0 V and the transistor enable relay opening to disable the output current. The corresponding error code is available through the terminal port, displayed using the Display Module, and sent to EPICS.

CONCLUSIONS

The modular design of the Trim Card II combats component obsolesce by allowing small daughter boards to be revised as needed. It also has shortened the development time by allowing sections to be designed and tested in parallel. More flexibility has been added by updating the microprocessor and adding a FPGA. Improved control and diagnostic features such as the transistor enable relay, thermal switch, Temperature Senor, Analog Monitor, terminal port, and Display Module are essential to easy troubleshooting. The design has been an overall success and will support accelerator upgrades in the future.

REFERENCES

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