THE APS SEPTUM MAGNET POWER SUPPLIES UPGRADE*

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Abstract

The higher requirements for beam injection stability at the APS storage ring (SR) demand improvement of pulsed power supplies for the septum magnets. The new specification for the current repeatibility is 1/2000. The upgrade will be performed in two stages. In the first stage we will implement a new voltage regulation circuit in the power supply with a new timing sequence that will provide better voltage regulation performance. A common design is made for all of the septum magnet power supplies (SMPSs) at the APS. The new regulation module has already been tested on both thin and thick SMPSs. The test shows that the achieved voltage regulation is much better than 1/2000. Combined with a current feedback loop, it can provide a shot-to-shot current repeatability better than 1/2000. The second phase of the upgrade will develop the current feedback loop and control algorithm. This paper will decribe the design and test results for the first phase only.

INTRODUCTION

There are six septum magnet power supplies at the APS – two for the booster beam extraction (B:ES1 and B:ES2), two for the SR beam injection (S:IS1 and S:IS2), one for the booster injection (PTB:IS), and one for PAR injection and extraction (PAR:PSP). The thin septa (S:IS2 and B:ES1) show no thermal effects when pulsing at 2 Hz for a long time. Thus voltage regulation appears to be sufficient for these power supplies. The thick septum magnet in the SR (S:IS1) has little thermal effect when operating in top-up mode by pulsing once every two minutes. The SMPS and magnet operate at ambient temperature equilibrium. During non-top-up operation and during studies, the septum magnet is operated at 2 Hz rate for about two minutes, a time frame in which most of the thermal effect occurs. The thick septum magnet in the booster (B:ES2) operates at a 2-Hz rate for a duration of 30 seconds to several minutes in all conditions: top-up and non-top-up operations, and studies. There is a constant thermal variation for this magnet and power supply.

The upgrade is a two-year project divided into two phases. In phase 1 the power supply is modified with a voltage regulation circuit, and new electronic control hardware is developed to accommodate a new regulation algorithm. Phase 2 will be devoted to the current feedback control to compensate for the thermal effect.

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POWER CIRCUITS

The Existing Circuit and Issues

The existing circuit for the SMPS is shown in Figure 1. It uses four SCRs to control the voltage across the capacitor bank C2 and discharge it into the septum magnet [1, 2]. This circuit has the following issues:

1. Voltage regulation in the existing circuit depends on the stability of the raw power supply (Lambda EMI), on the time jitter of charge command, and on a single comparison event in the control circuit, which is susceptible to EMI on the measured voltage signal.
2. There is a slow thermal drift in the peak current contributing to repeatability error. Current regulation is not provided in the hardware. The thermal effect compensation is done with a software script. For long-term stability, the thermal effect of the septum magnet needs to be compensated by a current feedback loop.
3. Electronics was built more than ten years ago and contains obsolete parts that are very difficult to maintain.

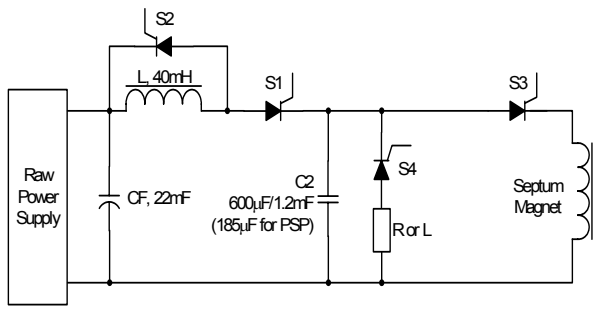

Figure 1: The existing switching circuit.

The New Circuit

Implementation of the voltage regulation algorithm requires changing the power switching circuit in the SMPS and employing electronics to control the circuit. The proposed solution is to install a voltage regulator between capacitor banks CF and C2. After comparing the buck and the boost configurations, we preferred a boost circuit because (1) V_{CF} can be one-half of V_{C2}, (2) there is less voltage stress on devices when V_{C2} reverses, (3) the circuit is easy to analyze, and (4) it's easy to design the regulator.

The following modifications have been made to the existing circuit: (1) S2 was removed from the charging choke, (2) S1 was replaced with D1 and IGBT1, and (3) IGBT2 and D2 were added to form a boost circuit with L, IGBT1, and D1. IGBT1 was needed to keep CF from being discharged during pulse. D2 was required to protect IGBT2 in case of an IGBT1 failure. The proposed circuit is shown in Figure 2.

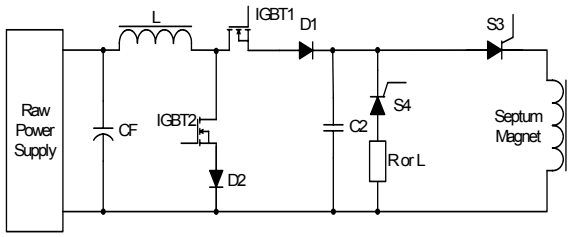

Figure 2: The proposed switching circuit.

There are five phases in the timing diagram shown in Figure 3.

- Discharge (t1 > t > 0): Thyristor S3 is triggered to discharge energy stored in the capacitor bank C_2 into the magnet;
- Reset (t2 > t > t1): Thyristor S4 is fired to bring C2 voltage to 0 or back to positive when energy recovery is necessary;
- Resonant charge (t3 > t > t2): IGBT1 is turned on, initiating the resonant charge of the C2;
- Boosting (t4 > t > t3): IGBT1 stays on and IGBT2 pulses with a fixed duty cycle, charging C2 until the voltage becomes higher than the set point Vref;
- Regulating (t > t4): IGBT1 stays on and IGBT2 pulses with a smaller duty cycle to regulate the voltage across C2.

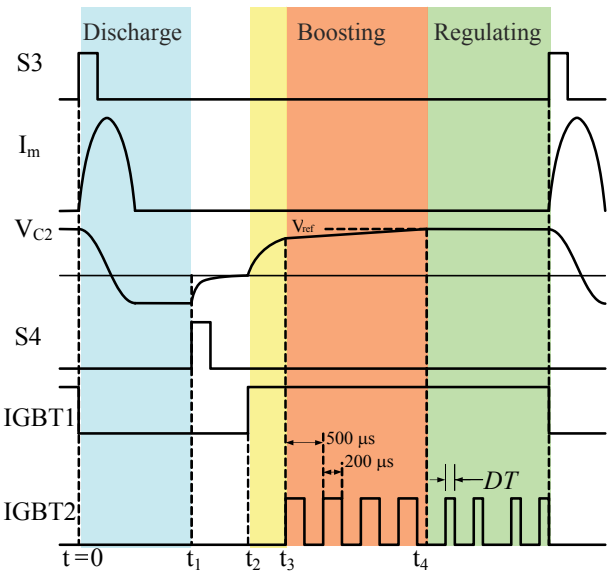

Figure 3: The timing diagram for the new circuit.

Equations

The on time (*DT*) for IGBT2 is the key parameter because it decides the ripple voltage of V_{C2}. To find *DT*, we use energy equations for L and C and the fact that the energy stored in the choke (L) has to transfer to C2 after each pulse. The following computation is based on the assumption that all devices are lossless.

After IGBT2 is on for *DT*, energy (E) is stored in L

$$E = \frac{1}{2}LI^2 = \frac{1}{2L}V_{CF}^2(DF)^2. \quad (1)$$

When IGBT2 turns off, energy goes into C2 and increases V_{C2} by ΔV:

$$E = \frac{1}{2}C_2\left\{(V_{C2}+\Delta V)^2 - V_{C2}^2\right\} = C_2V_{C2}\Delta V + \frac{1}{2}C_2\Delta V^2 \approx C_2V_{C2}\Delta V. \quad (2)$$

Since $\frac{\Delta V}{V_{C2}} \le \frac{1}{2000}$, Eq. (1) is equal to Eq. (2), and $V_{C2}=2V_{CF}$. The result after rearranging the equation is:

$$DT \le \sqrt{\frac{LC_2}{250}}. \quad (3)$$

Both the estimated and chosen *DT* values for each type of magnet are shown in Table 1.

Table 1: DT Values for Each Type of Magnet

	Max *DT*	Chosen *DT*
PAR (C2 = 185 mF)	172 µs	50 µs
Thin (C2 = 600 mF)	310 µs	100 µs
Thick (C2 = 1.2 mF)	438 µs	150 µs

Note: L = 40 mH for all cases.

$DT \approx DT_{max}/3$ is chosen because it provides a $\Delta V/V_{C2}$ almost ten times smaller than required by the specification, and it takes ten consecutive pulses to make DV/V_{C2} out of spec; therefore, the regulation can be more tolerable to noise. The timing values are shown in Table 2 for each of the six magnets.

Table 2: Timing Parameters for Different SMPSs at at the APS

	t_1 (ms)	t_2 (ms)	t_3 (ms)	t_4 (ms)	*DT* (µs)
S:IS1/B:ES2 (thick)	12 (ms)	165	190	V_{C2} dependent	150
S:IS2/B:ES1 /PTB:IS (thin)	1	150	180	V_{C2} dependent	100
PAR PSP (thin)	0.5	1	10	V_{C2} dependent	50

Since the boost circuit needs to operate in discontinuous mode to prevent excessive energy accumulation in the choke, which can cause a large step voltage change in C2 when IGBT2 is turned off before the discharge, the maximum duty cycle (*D*) has to be less than 0.5 (because $V_{C2} = 2\ V_{CF}$). One IGBT2 switching frequency that fits all circuits is

$$f_{\max} = \frac{1}{T} = \frac{D}{DT} = \frac{0.5}{150 \times 10^{-6}} = 3333(Hz). \quad (4)$$

The chosen frequency is 2 kHz.

Control Method – Bang-Bang Control

Bang-bang control is the simplest control algorithm and is inherently stable, fast, and easy to implement. Data processing is straightforward and control calculations are easily performed. This method is preferred in analog systems because design of digital controllers to compensate for sampling and quantizing errors due to noise sensitivity is more complex than analog systems of equivalent performance.

The algorithm works as follows: The capacitor bank voltage V_{C2} is continuously compared with the setpoint. If V_{C2} is less than the setpoint, IGBT2 is turned on for a fixed time (*DT)* to store energy in L, then IGBT2 is turned off, and the stored energy transfers to C2. V_{C2} increases by a ΔV after the energy transfer. This cycle repeats at 2-kHz frequency until V_{C2} reaches the setpoint. While V_{C2} is higher than the setpoint, IGBT2 pulses are not provided. The regulation continues until the discharge command is received.

Voltage Regulation Algorithm Implementation

The new power modules and control electronics have been designed and constructed to test the new algorithm. The control electronics comprises a voltage regulation module, an IGBT drive board, an SCR drive board, and snubber circuits for IGBTs. The voltage regulation module provides control signals for the power circuit with less than 10-ns jitter. A finite-state machine algorithm is implemented in EPM7128 (Altera Corp.) The module can be tuned to any type of SMPS at the APS. All electronics have already been tested on a thin and a thick SMPS in the test area. Figures 4 and 5 represent the measurements taken during the test. The test shows that the voltage regulation is much better than the spec of 1/2000.

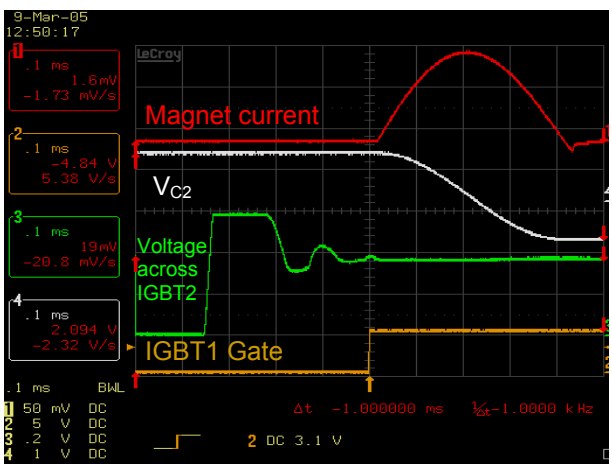

Figure 4: An oscillogram showing the magnet current shape during discharge.

Other Improvements

Attention has been paid to increase the signal/noise ratio when measuring the V_{C2}. The output of the isolation amplifier has been changed from single-ended to differential, which significantly reduced the 60-cycle component of noise in the V_{C2} signal. Ferrite toroids have been installed on the V_{C2} wires to reduce common-mode switching transients and other high frequency noise. The wiring layout in the cabinet has been improved with respect to crosstalk noise. The resulting data are shown in Fig. 6.

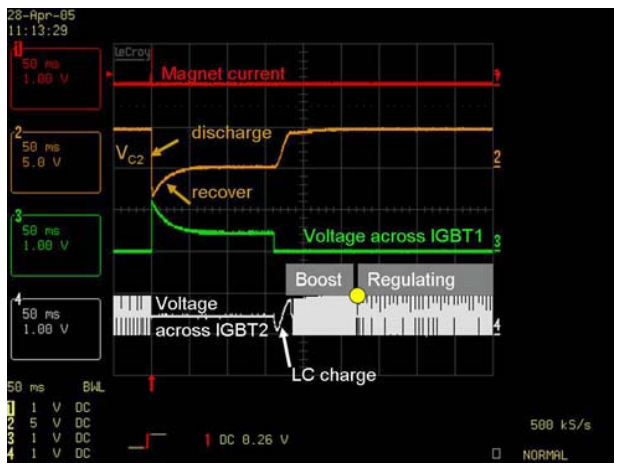

Figure 5: An oscillogram showing all stages of the capacitor bank charge/discharge.

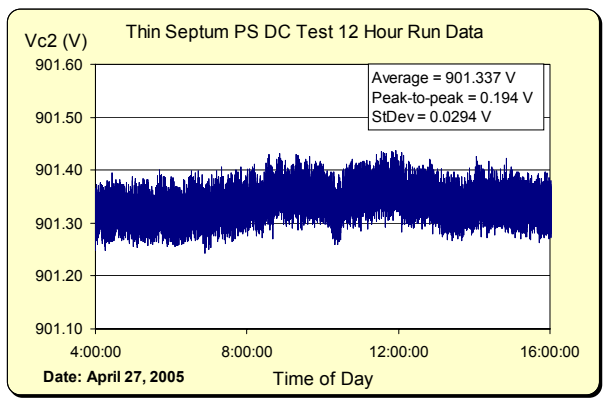

Figure 6: The capacitor bank voltage V_{C2} over time. Statistics are shown in the upper right corner.

ACKNOWLEDGEMENTS

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REFERENCES

[1] D. G. McGhee, "Pulsed Power Supply for PAR Injection/Extraction Septum Magnet," LS Note 159, September 23, 1990.

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