CONTROL LOOPS FOR THE J-PARC RCS DIGITAL LOW-LEVEL RF CONTROL

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Abstract

The low-level radiofrequency control [1] for the Rapid Cycling Synchrotron of J-PARC [2], [3] is based on digital signal processing. This system controls the acceleration voltages of 12 magnetic alloy loaded cavities. To achieve a short overall delay, mandatory for stable loop operation, the data processing is based on distributed arithmetic in FPGA. Due to the broadband characteristic of the acceleration cavities, no tuning loop is needed., The RF system operates simultaneously with dual harmonics (h=2) and (h=4) [4] to handle the large beam current. The stability of the amplitude loops is limited by the delay of low pass FIR filters used after digital down conversion. The phase loop offers several operation modes to define the phase relation of (h=2) and (h=4) between the longitudinal beam signal and the vector-sum of the cavity voltages. Besides the FIR filters, we provide cascaded CIC filters with smoothly varying coefficients [5]. Such a filter tracks the revolution frequency and has a substantially shorter delay, increasing the stable operating region of the phase loops. The adaptive radial loop samples the orbit variation. Combined with a feed-forward of the dipole current the effects of measurement errors on the effective acceleration frequency program are reduced.

THE CAVITY VOLTAGE LOOP

The digital cavity voltage loops exist individually for each of the (11+1) cavities at (h=2) and (h=4). The impedance of each cavity, where 3 acceleration gaps are in parallel, changes while the RCS revolution frequency sweeps from 469kHz to 836kHz. Therefore each voltage follows a pattern during acceleration. Figure 1 shows, for one cavity, how the gap voltage is sampled with 36MHz and then digitally down-converted at (h=2) and (h=4). The detected voltage is compared to a pattern. The difference is fed to a PID (Proportional, Integral, Differential) compensation function, shown in fig. 2. The PID output controls the amplitude for digital up-conversion. We provide 2 operating modes: pattern and PID output can be are added or multiplied. Limiter functions prevents overflow when the feedback signal is missing. Finally the (h=2) and (h=4) signals are combined and fed to the transistor amplifier which drives the push-pull tube amplifier that delivers the RF power to the cavity and the acceleration gaps. For stability of the loop, the 14µs delay of the symmetric FIR low-pass with 63 filter-taps, downsampled at 9MHz is dominant. For a linear ramp, the FIR output follows the input with a delay of approximately 7µs. All arithmetic functions are realized with FPGA on 9U VME (fig. 3) for high throughput data rate. Before implementing, the functions are simulated with SCILAB and Spice.

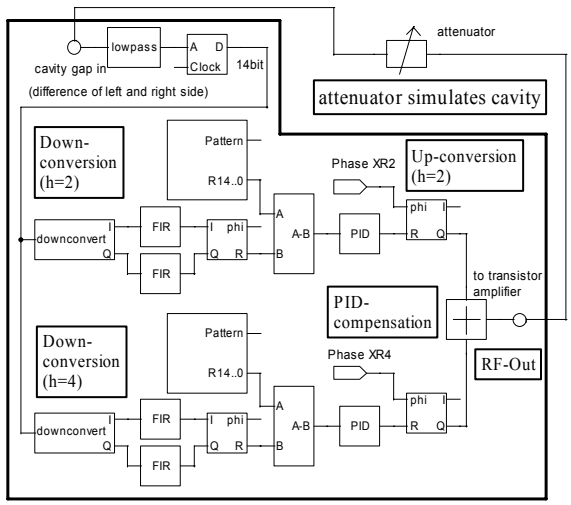

Figure 1: Cavity voltage loop – attenuator simulates cavity.

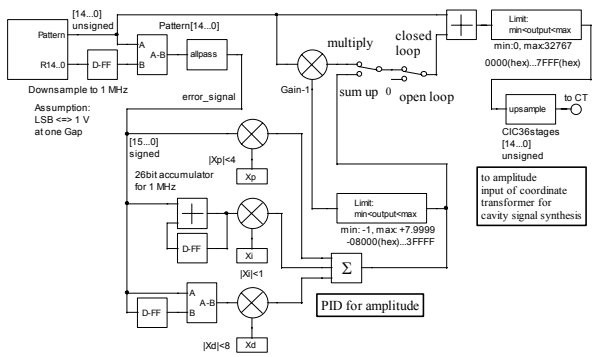

Figure 2: PID-amplitude controller.

Figure 3: RFG (radio frequency generation) board.

Amplitude Loop Test

Figure 4 shows the error signal of the amplitude controller for PID settings Xp=1, Xi=0.2, Xd=0. After the "reset" from 25Hz trigger, which appears before each RCS-cycle, the integrator for the integral part starts from

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Zero. This is equivalent to the response to a step in the amplitude pattern. For this test, the RF-output of the RFG-board was connected with an attenuator to the cavity measurement input. The signal frequency was 1MHz at (h=2). Figure 5 shows the stability limit. When the external attenuator between "RF-out" and "cavity-in" is changed from –6 to –5 dB, the loop becomes unstable, and oscillates at approximately 18kHz. This frequency is related to the delay in the FIR filter. The total loop gain is a product of all transfer functions in the amplitude loop. The stability of the loop with the cavity is checked for the highest gain on the analogue path from amplifier input to cavity output.

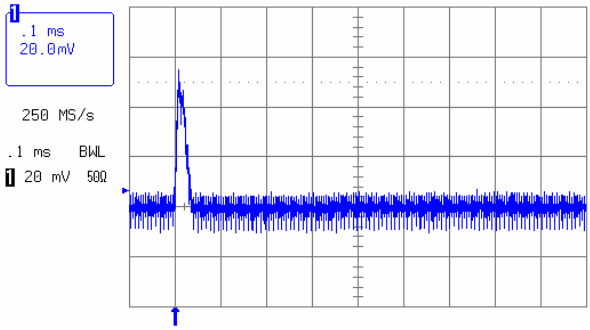

Figure 4: The closed loop is stable for Xp=1, Xi=0.2, Xd=0. The error signal returns to zero without ringing.

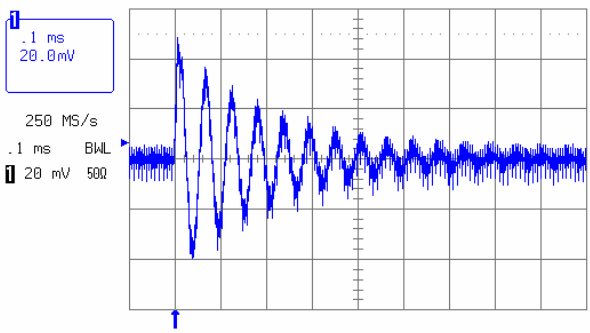

Figure 5: The amplitude loop is near un-stability for Xi=0.5 and –6dB outer attenuation.

With Xp=Xd=0 and Xi=0.1 the stabilizing effect of the amplitude control loop in the mode "pattern added to PID-output" was verified.

The RF-out pattern was set to constant 8191=125mV amplitude. If there were no losses in the analogue part of the cavity-input, the 2Vpp would be equal to a full-scale digital measured amplitude R2=32767. For calibration, a signal with 2.3Vpp was applied, that results in a digital amplitude at (h=2) slightly below R2=32767. The expected digital value R2=8191 is equal to an analogue input signal of approximately 580mVpp. Figure 6 shows, that for attenuator settings between –1 and –4 dB, the cavity input voltage is held constant by the amplitude loop, which adjusts the signal at RF-out. The signal at RF-out is limited to 990mVpp. Therefore if the attenuator setting is -5 or -6dB, the output is saturated and cannot generate the voltage that would be required to keep the level at "Cavity-in". It was confirmed, with a smaller pattern value, or with more gain, when the amplitude controller is connected to the combination of tube amplifier and cavity, the control margin increases accordingly.

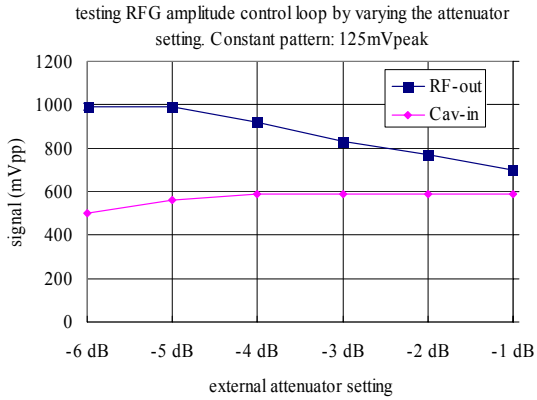

Figure 6: Testing the amplitude loop with constant pattern – the cavity measurement input voltage is kept constant.

THE PHASE LOOP

The beam phase loop controls the phase between the phase and gain compensated vector-sum of the (11+1) cavity voltages (fig. 7) and longitudinal beam signal monitored with FCTs (fast current transformers). The acceleration phase at (h=2) and the phase for the bunch shape manipulation (h=4) follow patterns. The digital receiver for the longitudinal beam signal is shown in figure 8. With a phase compensation pattern, ambiguity of the phase average of the two FCTs is avoided. Several modes for dual-harmonic operation are foreseen (figure 9), for example:

- (h=2) and (h=4) are independent
- (h=2) is master, and (h=4) follows (h=2).

All 4 phase measurement signals, e.g. beam and cavity for (h=2) and (h=4) can be inverted. In case, DC coupling of the phase loop results in an over-determined system, a DC-cut high pass with variable cut-off is foreseen.

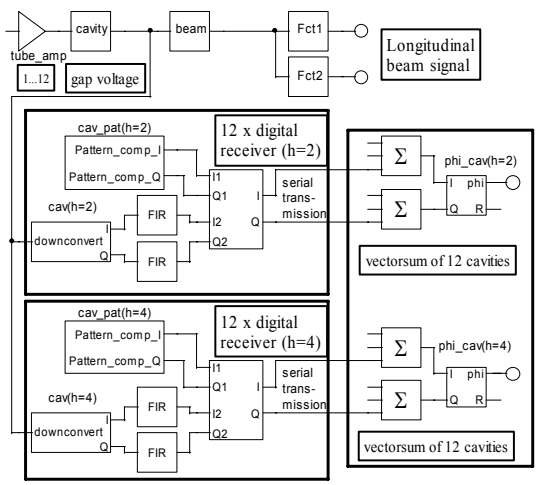

Figure 7: The vector sum of up to 12 cavity voltages.

The phase loop damps synchrotron oscillation by providing a damping term with 90º-phase shift. During the

20ms acceleration time will be approximately 55 synchrotron turns - the last turn at 18ms. All oscillations have to be damped before, so that a stable beam can be transferred either to the MR (Main-Ring) or to the MLF (neutron target). The FIR low pass filter mentioned before allows damping of synchrotron oscillations up to 18 kHz. We have developed a different type of digital low pass filter [5] that reduces the delay by 50% and increases the stability margin. The filter structure, shown in fig. 10, is based on linear approximation between 2 CIC filters with variable coefficients tracking the RCS revolution frequency. Such filters are known for a variable clock operating on a multiple of the revolution frequency [6]. Here, we use linear interpolation between one notch-filter above and a second notch-filter below the accelerator revolution frequency. Simulation shows, that the loop is stable for synchrotron frequencies up to 30kHz and may provide damping within 100μs.

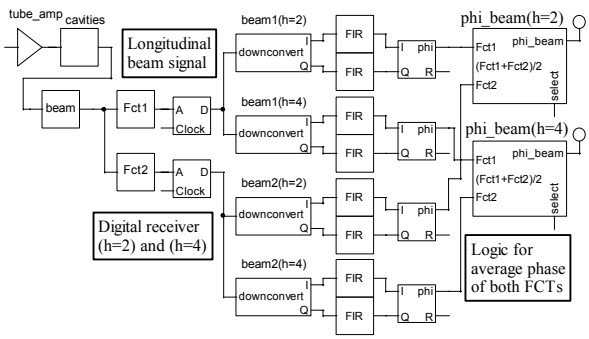

Figure 8: Processing longitudinal beam phase signal.

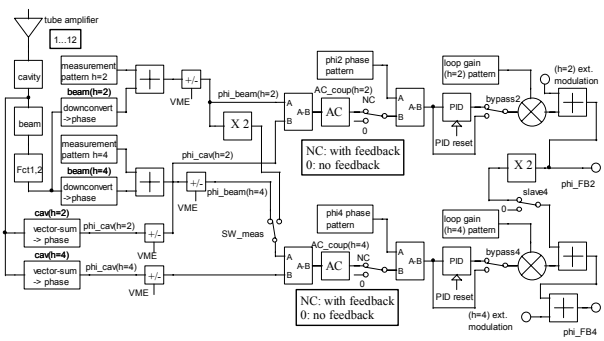

Figure 9: Selection of dual harmonic operation mode.

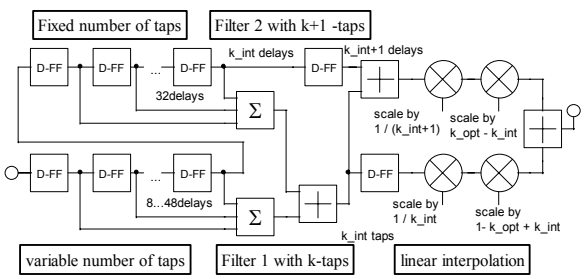

Figure 10: Digital low pass based on a CIC structure.

ORBIT CONTROL

The dipole magnet current is averaged (linear or exponentially) up to 8000 cycles for feed forward to compute a frequency offset Δf_B for the main synthesizer (SPG-board). The feed-forward is adjusted by a gain pattern and a hysteresis correction pattern. The radial loop controller shown in figure 11 averages the position signals from 3 BPMs and computes the frequency offset Δf_R. For each BPM input a fixed DC value for offset compensation can be set. The weighting function for each BPM allows selecting, which BPM is used (Zero weight = unused). The measured orbit variation during a cycle and the resulting frequency pattern that was used by the synthesizer

$$f_{rev} = f_{prog} + \Delta f_B - \Delta f_R \quad (1)$$

are stored in onboard-memory. They are analyzed for adaptive modification of the frequency pattern and setting of loop gain pattern and PI coefficients for the radial loop. The gain pattern includes compensation of dispersion effects. Setting entries in the gain pattern to Zero switches the radial loop off, which is helpful for optimisation.

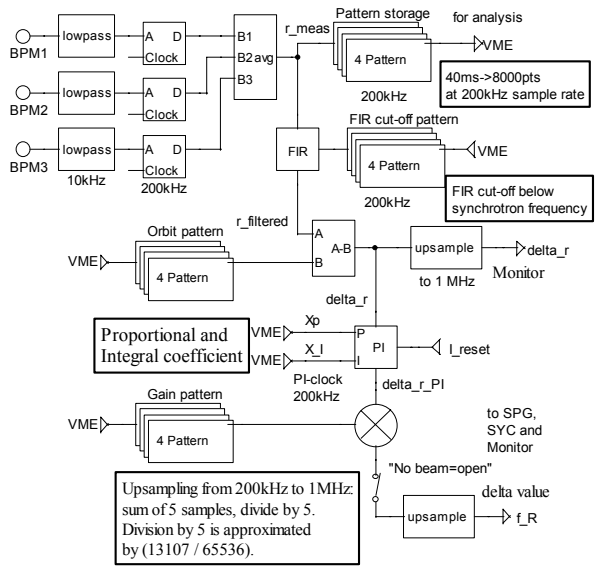

Figure 11: averaging orbit of 3 BPMs for frequency offset.

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