THE DIGITAL FEEDBACK RF CONTROL SYSTEM OF THE RFQ & DTL1 FOR 100MEV PROTON LINAC OF PEFP*

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Abstract

The 100 MeV Proton linear accelerator (Linac) for the PEFP (Proton Engineering Frontier Project) will include one RFQ and one DTL1 at 350 MHz as well as seven DTL2 cavities at 700 MHz. The low level RF system with the digital feedback RF control provides the field control to accelerate a 20mA proton beam from 50 keV to 20 MeV with a RFQ and a DTL1 at 350 MHz. The FPGA-based digital feedback RF control system has been built and is used to control cavity field amplitude within ± 1% and relative phase within ± 1º. The fast digital processing is networked to the EPICS-based control system with an embedded processor (Blackfin).

INTRODUCTION

The PEFP accelerator has been designed to accelerator a 20 mA proton/H- with the final energy 1 GeV. The 20 MeV proton accelerator is being constructed in the PEFP test facility, and will be commissioned in 2005. After the commissioning, PEFP test facility will provide the proton beam for the many industrial applications. With the technologies developed in PEFP test facility, the 2nd phase accelerator of 100 MeV energy will be constructed in 2010.

In the 100MeV proton linear accelerator (LINAC) for PEFP, the RF source will power two-accelerator cavities (an RFQ, a DTL1) operated at a frequency of 350 MHz, and seven cavities (DTL2) operated at frequency of 700 MHz. Presently it aims to achieve 100 MeV beam energy with 20 mA(peak, 1-mSec macro-pulse duration) beam current. Refer to Table 1 for major beam parameters of the PEFP accelerator.

Table 1: Beam Parameters of PEFP/KAERI Accelerator

	Operation Mode	**NOTE**
	Pulse	
Beam Energy	3 – 20 – 100MeV	BPM Operation Region
	0.08 – 0.20 – 0.43	
	1.003 – 1.021 – 1.107	
Average Beam Current(I_{av})	Peak 20mA	
Pulse Width	Few mSec	
Bunch Length	160pSec	PARMILA Simulation Result
Bunching Frequency	350MHz	

We are developing the digital feedback RF control system based on recent digital technology available for the better performance. One of the advantage of the on-going digital feedback control system is to take mainstream solution using a FPGA & an embedded Processor. The digital feedback RF control system for 100 MeV proton linear accelerator provides field control including an RFQ and a DTL at 350 MHz as well as 7 DTL cavities at 700 MHz. In our system, an accelerator electric field stability of ± 1% in amplitude and ± 1º in phase is required for the RF system. The digital RF feedback control system using the FPGAs and DSP Embedded Processor is adapted in order to accomplish these requirements and flexibility of the feedback and feed- forward algorithm implementation. In addition to field control, it provides cavity resonance control, and incorporates the personnel and machine protection functions.

OVERVIEW

All devices including the digital feedback RF control system for each accelerators (RFQ and DTL1) are installed in a 19" shielded rack, 40U high, 800 mm deep together with the beam position monitor electronics and the event trigger system for pulse operation of the PEFP proton LINAC. The accelerator RF source (klystron driving signal) of 350 MHz is generated by a VCO PLL synchronizing with the distributed 10 MHz reference. The low level RF system consists of three 19" rack-mount chassis; a digital feedback RF control system, a coupled RF signal distributor for appropriate distribution, ac power line conditioner with noise cut transformer.

DIGITAL RF FEEDBACK HARDWARE

The digital feedback RF control system is a perfect all-in-one type. A single 4U high 19" shielded enclosure contains all components with dedicated linear power supplies. Most of the analog and digital processors including DSP embedded processor are included on the digital feedback RF control board as shown figure 1. We have developed the digital feedback RF control system through three times changes in order to obtain good performance for two years. The four 14-bit ADCs (AD6644) operated at 40 MS/s, and two 14-bit DAC (AD9744) operated at 80 MS/s. Xilinx XC3S1500FG676 (changed from XC2V1000FG256) FPGA provides signal processing path, and connects to an 400MIPS DSP embedded processor (Analog Devices's Blackfin ADSP-BF532SBST400. The digital feedback RF control system relies on FPGA (Field Programmable Gate Array) and digital signal processors optimised for real-time signal processing. The digital feedback RF control system performs feedback and feed-forward algorithms on the

field signal, resulting in control inphase and quadrature (I/Q) outputs, which are processing DSPs (Digital Signal Process) for slow and complicate processing. The total feedback loop delay is considered to be less than 1uS, including all of the RF components, cables, ADCs, DACs and FPGAs. The digital feedback RF control system is relatively complex as shown in figure 1.

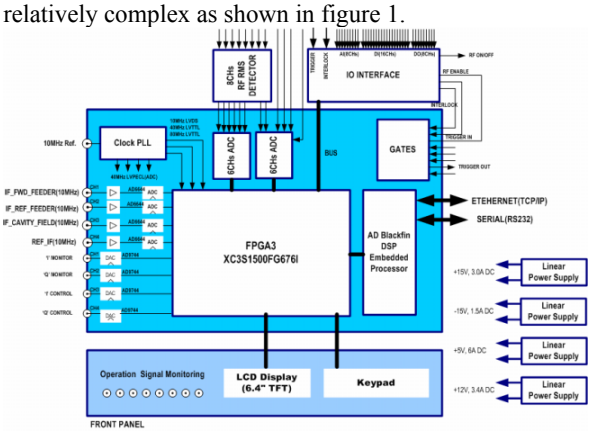

Figure 1: The detailed configuration of the digital feedback RF control system.

The phase lock loop circuitry, base on an PLL IC (Analog Devices's ADF4001) can lock the on-board voltage controlled crystal oscillator (VCXO, 80 MHz Connor-Winfield VPLD54TE) to an external source. In our case, that source is a 10MHz master oscillator signal.

A synchronized clock signal (80 MHz LVPECL) generation is serially-programmed to accommodate the optimised clock signal frequency. The RF amplitude and phase resolution depend on the ADC sampling clock jitter relative to the various RF sources in the system. Figure 2 shows the performance of the PLL clock generator on the digital feedback RF control board.

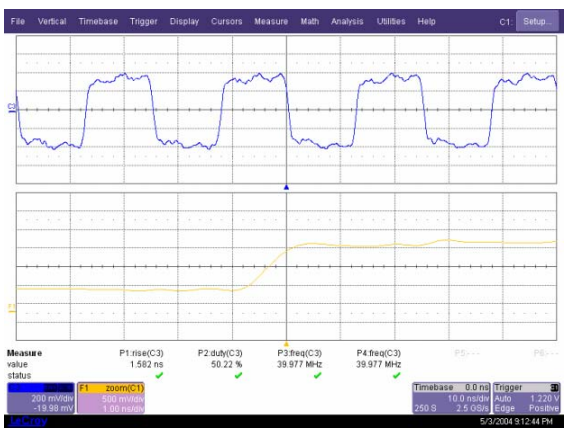

Figure 2: The characteristics of the PLL clock generator.

The control parameters are set through the MODBUS controller such as a single computer or the controls using the keypad and the touch pad on the screen to set up the LLRF system, in the various ways. Registers on the module provide to access for all manners of control – set points, thresholds, mode selection, controller type, etc, and the DSPs provide the direct interface to the control register and hardware. Timing and interlocks are routed through an FPGA. Hard-wired interlocks provide positive cut off of the RF drive in case of external fault conditions. This feature is purposefully independent of the FPGA and DSP embedded processor.

Figure 3: The photograph of the digital feedback RF control system.

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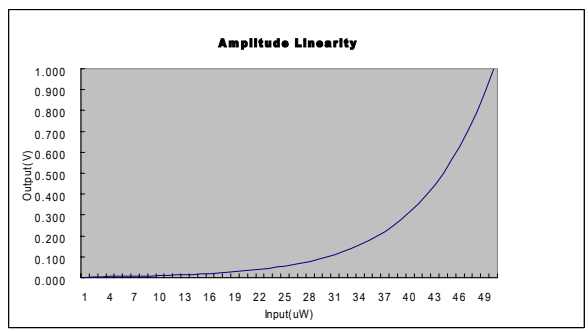

Figure 4: RF signal (350MHz Carrier) amplitude linearity of the digital feedback RF control board.

Figure 4 shows the amplitude sampling linearity of the carrier signal to be induced from the low level RF system output. Figure 5 shows the configuration of the interface between the LLRF system and the EPICS IOC. MODBUS TCP protocol is selected for communication at the LLRF digital RF feedback control. The local test of the LLRF system is going to use lookout software at personal computer basis on windows OS as shown figure 6. And EPICS control system will be connected to confirm the performance of the LLRF system on local condition.

The non-linear dynamics of a single RF cavity can be represented by the state-space equation:

$$\frac{d}{dt}\begin{bmatrix} V_I \\ V_Q \end{bmatrix} = \begin{bmatrix} -\omega_{1/2} & -\Delta\omega \\ \Delta\omega & -\omega_{1/2} \end{bmatrix} \begin{bmatrix} V_I \\ V_Q \end{bmatrix} + \frac{\omega_{rf}}{2}\frac{R}{Q}\begin{bmatrix} I_I \\ I_Q \end{bmatrix},$$

where $\omega_{1/2} = \omega_{rf} / 2Q$ is the half width of the resonance, $\Delta\omega = \omega_0 - \omega_{rf}$ the cavity detuning, and ω_0 the resonance frequency of the cavity.

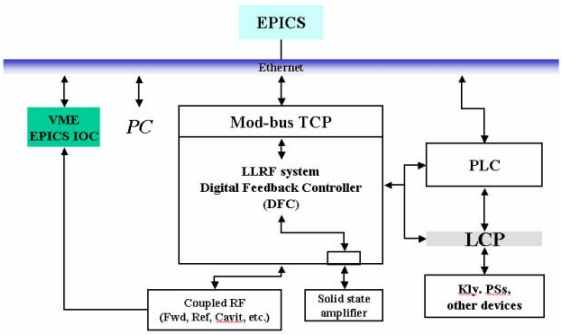

Figure 5: The basic interface configuration between the LLRF system and EPICS control system.

In order to test the low-level RF system in a lab, a simulation RF cavity with the similar RF properties to the RFQ was made. The cavity is a quarter-wave resonator structure of which the resonance frequency is 350 MHz and the unloaded Q-value is 8,000. The cavity can withstand about 100-W CW RF power so that the test condition almost same with a hot RFQ cavity can be realized except a high power klystron tube.

SUMMARY

We are ready to test the performance of the digital RF control system in the lab with a simulation to be made and the MODBUS controls, and will be given a chance to try it out on a real RFQ and DTL1 at PEFP test facility in June 2005. Further improvement of the performance is being studied.

ACKNOWLEDGMENT

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