STATUS OF THE RF BPM UPGRADE AT THE ADVANCED PHOTON SOURCE*

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Abstract

The Advanced Photon Source (APS), a third-generation synchrotron light source, has been in operation for eleven years. The monopulse radio frequency (rf) beam position monitor (BPM) is one of three BPM types now employed in the storage ring at the APS. It is a broadband (10 MHz) system designed to measure single-turn and multi-turn beam positions, but it suffers from an aging data acquisition system. The replacement BPM system retains the existing monopulse receivers and replaces the data acquisition system with high-speed analog-to-digital converters (ADCs) and a field-programmable gate array (FPGA) that performs the signal processing. A first-article system has been constructed and is currently being evaluated. This paper presents the results of testing of the first-article system as well as the progress made in other areas of this upgrade effort

INTRODUCTION

The planned upgrade of the rf BPMs at the APS will replace only the data acquisition portion of the system. This will be accomplished by physically separating the existing monopulse receiver from the signal conditioning and digitizing unit (SCDU) [1] data acquisition electronics and repackaging the receiver in a custom EMI-shielded chassis and replacing the SCDU with a new custom data acquisition module in a C-sized VXI form factor. This will allow for a future upgrade to the receiver if desired.

We are following a three-phase program in this effort because of the critical nature of the system. In the first phase we developed two channels of data acquisition using a custom designed, dual ADC board and an Altera Stratix® II development kit [2]. The ADCs used are Analog Devices [3] AD6645, 14-bit 105 MSPS devices. The second phase is the development of a C-sized VXI module with eight ADC channels of data acquisition, together with the Stratix® II device. In this phase, we will instrument seven BPMs in one sector. The third phase will instrument the remaining storage ring sectors.

DESIGN OVERVIEW

The capacitive button pickups, matching networks [4], filter comparator, Heliax® cables, and monopulse receiver are all carried forward from the existing BPM system. We designed a customized 8-slot EMI chassis to house the monopulse receivers. We also designed an aluminum block on which we will mount the monopulse receiver. This aluminum block acts as both a heat sink and a guide for sliding the module into the chassis. On the reverse side of the aluminum block is a receiver interface circuit board. This circuit board mates with the receiver and provides power supply filtering and regulation for the receiver, drive circuitry for buffering the video signals from the receiver to the data acquisition board, buffers for digital control of the receiver, and a self-test circuit.

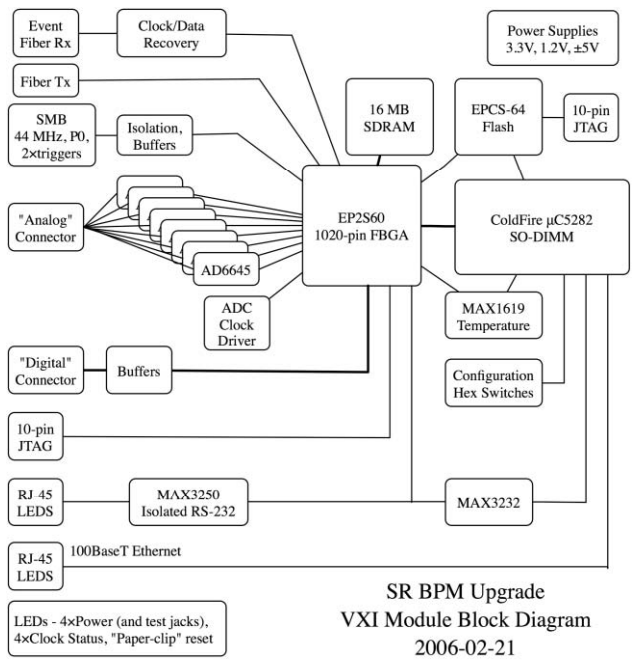

Figure 1: Block diagram of the BSP100 VXI module.

The BPM signal processor (BSP100) data acquisition board, a single-width C-size VXI module shown in Figure 1, replaces the old SCDU data acquisition system. Each module receives position and intensity data from four BPM receivers. On the module are eight high-speed, 14-bit ADCs running at 88 MSPS synchronized to the storage ring rf frequency. The FPGA reads the digitized signals and performs digital filtering and additional signal processing.

The FPGA firmware consists of five major functional blocks, namely an APS-developed timing system receiver block, an acquisition control block, a preliminary processing block, a continuous-processing block, and a triggered-processing block.

The timing system receiver handles all the synchronization of the system from the APS timing system. It also contains the standard APS event receiver functionality for use by the triggered-processing block.

The acquisition control block drives the plane-select and commutation switches within the monopulse

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receivers and directs the acquired samples to the appropriate processing blocks. The preliminary processing block reads from the ADCs and computes the single-turn average of the sum and position signals from each of the monopulse receivers. The continuous-processing block linearizes and filters the turn-by-turn signals and forwards the appropriate values to the fast-feedback and orbit-control systems, as well as to any other experimental physics and industrial control system (EPICS) clients. The triggered-processing block provides data acquisition capabilities [5] for machine studies or post mortem analysis. Additional details regarding this design can be found in references [6] and [7].

DESIGN STATUS

Since the last report [8], progress has been made in several areas, including chassis development, hardware design, engineering software, and application software. Performance tests are currently being conducted with good results. Lab data taken to date have demonstrated performance similar to our two-channel prototype unit. This portion of the paper will discuss our progress with the hardware and software development.

Chassis Development

In order to reduce the overall system weight, ease of installation, and maintenance, two separate chassis have been developed to provide housing for receiver modules and power supplies. Both chassis are standard 4U height by 19" wide and are capable of providing EMI shielding of 50 dBm at the fundamental frequency of 351.94 MHz. The receiver chassis contains a custom-built backplane, which provides power and interface to the BSP100 VXI card for a total of eight plug-in receiver modules. Each BSP100 VXI card provides control and data acquisition for up to four receiver modules. The power supply chassis, containing four separate linear power supplies, provides all the required voltages to the receiver chassis via a multi-conductor shielded cable.

A fan tray was designed to sit atop the receiver chassis to draw heat away from the receiver modules. The front and rear of the receiver chassis are closed so that a constant flow of cool air will be drawn from bottom to top.

These two chassis have been built and thoroughly tested in the lab. Two additional chassis sets are being assembled for installation in the storage ring.

BPM Signal Processor

The BPM signal processor (BSP100) has been designed, built, and functionally tested in the lab. This design has all the functionality of our two-channel prototype but with eight total ADC channels. The first board is now being integrated with the receivers and system testing is ongoing. A second layout has been approved and sent out for manufacture.

Feedback Interface

With the development of the new BPM system, we needed to upgrade our interface to the feedback system. The old BPM system provided 271 kHz, turn-by-turn raw data from each BPM to a separate board, which filtered and processed the data for use by the feedback system. The new system will filter and process the data from each BPM on board the BSP100 before sending the 600 Hz bandwidth data at a 135 kHz rate to the feedback system for immediate use.

The new interface functions predominantly as a data collector. Each board will reside in the feedback input/output controller (IOC) VME crate and collect the data from two BSP100 boards via fiber interface. The data is provided to the feedback system via the VME bus.

Software

EPICS device support and a database have been developed and are being used for testing and characterization of the system. Care was taken to replicate, as much as possible, the process variable names used in the current system. There are, of course, new process variable names for the additional functionality provided by the new design.

Engineering software necessary to control and monitor the BSP100 configuration, a Tcl/Tk application, was developed to set up and configure the module. Some of the controls include X/Y plane selection, 0/180 selection, number of samples per bunch, number of bunches per turn, trigger source selection for event triggering, and number of pre/post trigger samples for the post mortem history function.

Several default configurations associated with the various bunch fill patterns available at the APS have been established for operations use.

Test Results

System noise was re-measured to ensure that the noise level is approximately the same as the two-channel prototype unit. For this measurement, the receiver module's position inputs were terminated with 50 Ω terminators; a 0 dBm, 351.927 MHz, continuous wave (cw) signal was injected into the intensity input; and 262144 sample points were collected at the revolution frequency of 271 kHz. The results of the system noise test are shown in Figure 2. The conversion to microns is based on the standard elliptical storage ring chamber. If the 8mm chamber is used, the noise measurement improves by a factor of 6.5.

Among the enhancements provided by the new BSP100 are new process variables for band-limited rms power. A power sweep of the BPM system was performed and data collected from these new process variables. Figure 3 shows the results of this experiment with our standard chamber dimensions assumed.

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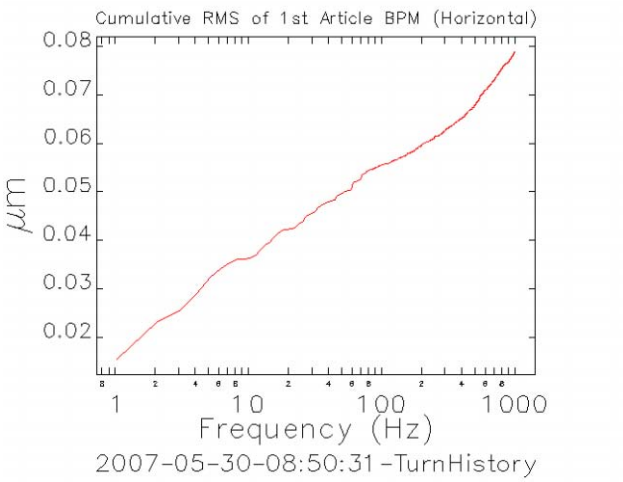

Figure 2: PSD of the BPM system noise for one channel.

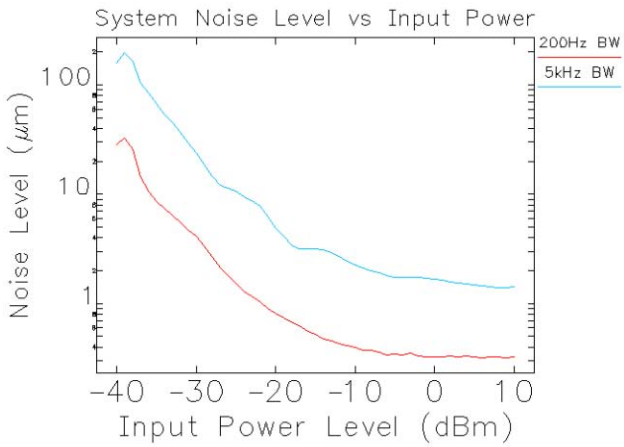

Figure 3: 50 dB power sweep of the BPM system showing the resultant noise levels of the position reading of 330 nm in a 200 Hz bandwidth and 1.7 μm in the 5 kHz bandwidth.

SUMMARY

We have begun evaluation of the first-article prototype of the monopulse rf BPM upgrade for the APS. The upgrade retains the existing monopulse receivers and replaces the data acquisition system with high-speed ADCs and an FPGA that performs the signal processing.

This paper discussed the progress made towards implementing our phase II goals for the prototype rf BPM for the APS storage ring. Testing has shown that the first-article prototype performs as well as our initial, two-channel version and does indeed meet or exceed the specifications set forth for this system. Special attention was given to cooling of the receiver chassis as this is where most of our thermal drift will originate. Long-term stability testing will take place in the near future.

We are encouraged by our results and look forward to completing the second phase of this project, at which time we will be able to demonstrate an improvement in orbit stability.

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