DEVELOPMENT OF DIGITAL TRANSVERSE BUNCH-BY-BUNCH FEEDBACK SYSTEM OF HLS

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Abstract

Hefei Light Source (HLS) operates at high beam current with many bunches. Multi-bunch instabilities degrade beam quality. An FPGA based digital transverse bunch-by-bunch feedback system was under development in HLS to suppress beam instabilities. The design of the digital feedback system and primary experiment results are presented in this paper. Further improving of the feedback system and investigating of the characteristics of the feedback loop are the future work.

INTRODUCION

HLS is a synchrotron light source，injecting in the energy of 200MeV and operating in the 800MeV at 200-300mA with a circumference of 66 meters. It operates with 45 bunches in 204.016MHz RF. A multi-cycle multi-turn injection system is used for current accumulation. A wiggler is available in the HLS. The range of horizontal tune of HLS is from 3.54 to 3.56, and the range of vertical tune is from 2.56 to 2.58 for user operation.

An analog transverse bunch-by-bunch feedback system of HLS has been developed [1], using two BPMs (Beam Position Monitor) and one kicker, which was under commissioning since last year. The digital transverse bunch-by-bunch feedback system of HLS, using only one BPM and one kicker, enlarges the tune acceptance and improves damping ability of multi-bunch instabilities with high order FIR filter.

THE TRANSVERSE FEEDBACK SYSTEM

Two digital signal processing boards with 102MHz (RF/2) clock system are used to process the bunch-by-bunch signal. The bunch number of HLS is 45, an odd number, which is impossible to be processed in one turn of the ring using two boards. Two turns of beam signal are treated as one turn signal with harmonics of 90.
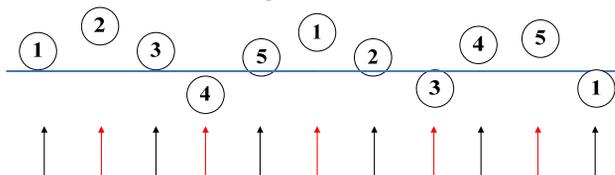

Figure 1: The Scheme of Digital Feedback Using Two Boards

The scheme of digital feedback using two boards is shown in Fig.1, which is a case of 5 bunches. Black arrow

represents sampling by one board and the red arrow represents the other board. 45 bunches in HLS is the same case that every board deals with all 45 bunches in two turns.
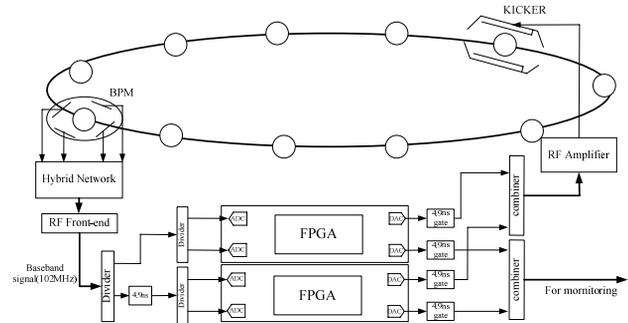

Figure 2: Overview of HLS Digital Transverse Bunch-by-Bunch Feedback System

The overview of HLS digital transverse bunch-by-bunch feedback system is shown in Fig.2. It consists of a BPM, a RF front-end, two digital processing boards, a RF amplifier and a kicker. The base-band bunch-by-bunch signal from the RF front-end is processed in two digital processing boards which calculate the correction kick signals for each of these bunches independently. The correction signals being amplified by a RF power amplifier are applied to the kicker. A new transverse kicker equipped in April was used to damp the beam instabilities.

Front-end

The beam signals from four button pickups of a BPM are combined in a hybrid network, producing X, Y and I signals. These signals are demodulated into base-band by an RF front-end working at a central frequency of 612 MHz.
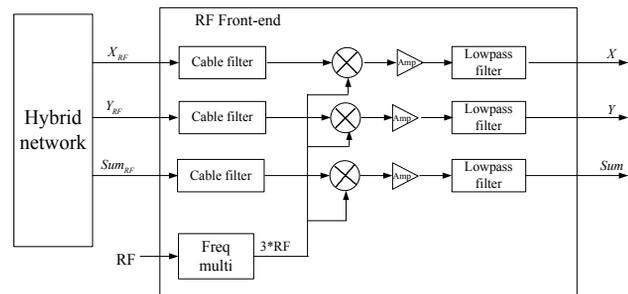

Figure 3: Layout of RF Front-end

The front-end of digital feedback system is shown in Fig.3, which is also part of bunch-by-bunch measurement system [2].

Digital processing boards

The digital signal processing modules for feedback, offered by SPring-8, are based on Hunt engineering HERON IO-2V ADC-FPGA-DAC boards. Each board is composed of one FPGA (Xilinx XC2V1000-4, 1MS/s) for digital signal processing, two 12-bit ADCs (AD9432, 105MS/s) and two 14-bit DACs (AD9767, 125MS/s) [3]. A 10-tap FIR filter is implemented in the FPGA. Limited by the resource of FPGA, one ADC and one DAC of each board are not used for feedback, but for monitoring. The feedback processor is operated at 102 MHz, which is half of the RF of HLS. Each ADC samples once every two bunches and two ADCs cover all bunches. Then a combiner is used to multiplex two channels of feedback signal.
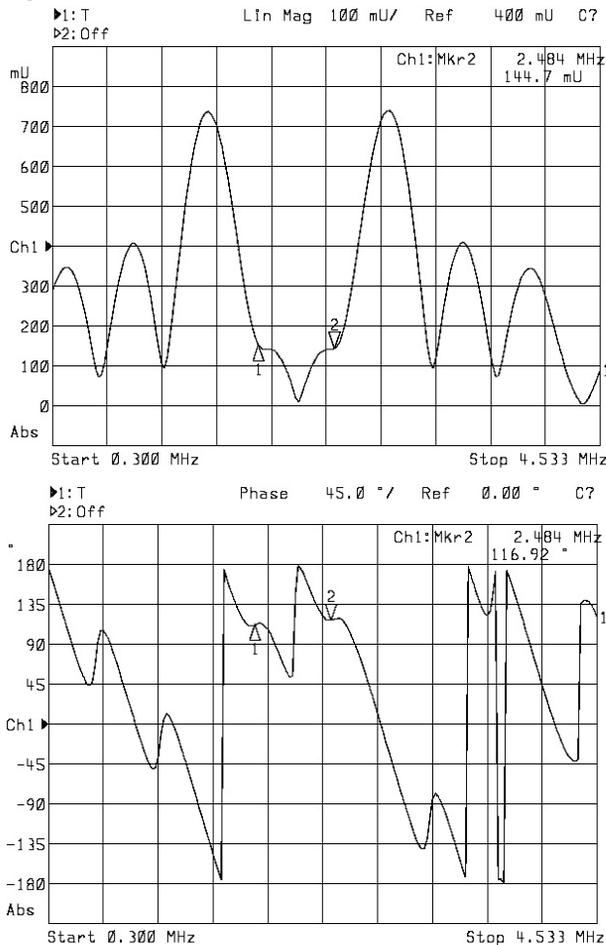

Figure 4: Frequency Response of the 10-tap FIR Filter Measured by the Network Analyser

Time domain least square fitting method, developed by T. Nakamura [4], was applied to the configuration of 10-tap FIR filter. Only one dimensional transverse feedback was carried out in single loop of the feedback system, and the FIR filter was designed for one turn with harmonics of

45. Fig.4 shows the frequency response of the FIR filter measured by the network analyser. The marker2 in Fig.4 pointing 2.484MHz is the revolution frequency timing 0.548 which is the fractional tune of horizontal direction. The upper plot of Fig.4 is the amplitude response and the lower one is the phase response. The FIR filter rejects the revolution frequency, and compensates the phase advance between the BPM and the kicker.

Clock system

The transverse feedback system relies on a very strict timing system. The two digital processing boards operate in 102MHz (RF/2), and DACs output two 9.8ns width feedback signal simultaneously. To get the feedback signal for kicker, the 4.9 ns width gates are used to switch the outputs of two boards. Double balance mixers (DBM) are used as switch gates.
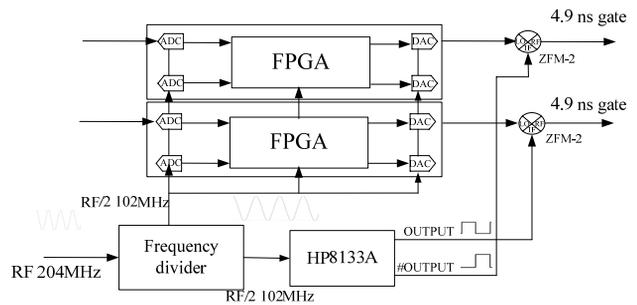

Figure 5: Clock System of Digital Feedback System

The clock system of digital transverse feedback system, which is shown in Fig.5, consists of a frequency divider (IDT5V9885) and a pulse generator (HP8133A). Frequency divider outputs RF/2 (102MHz) frequency signal to digital signal processors and HP8133A. HP8133A outputs two opposite 102MHz, 0V ~1V square wave signals, which are sent to the IF of DBMs to form 4.9 ns width switches.
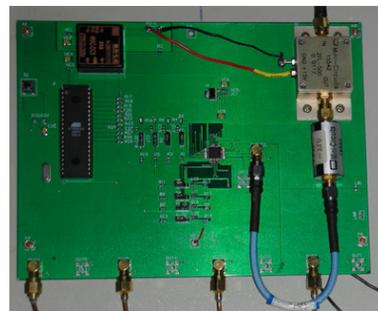

Figure 6: Frequency Divider Circuit

Frequency divider circuit, which is shown in Fig.6, is used to generate RF/2 frequency from RF signal in digital feedback system. IDT5V9885 is a programmable clock generator with three internal PLLs, which can generate three independent frequencies from the same input signal. The frequency divider is used in digital feedback system, and also used in the RFKO system which is shown in Fig.7.

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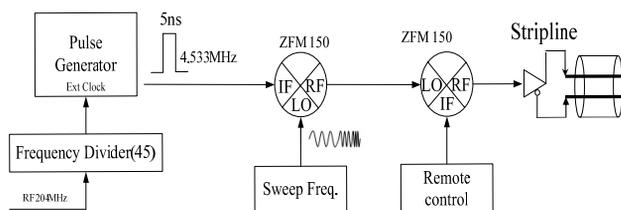## RESULTS OF PRIMARY EXPERIMENT

Delay adjusting

Figure 7: RFKO System to Form Single Bunch

To adjust the whole system delay of digital feedback system, a RFKO system was used to form single bunch, which is shown in Fig.7. Sweeping frequency combined with a 5 ns width gate in the frequency of 204MHz (RF frequency) kept one bunch, knocking out the other 44 bunches.
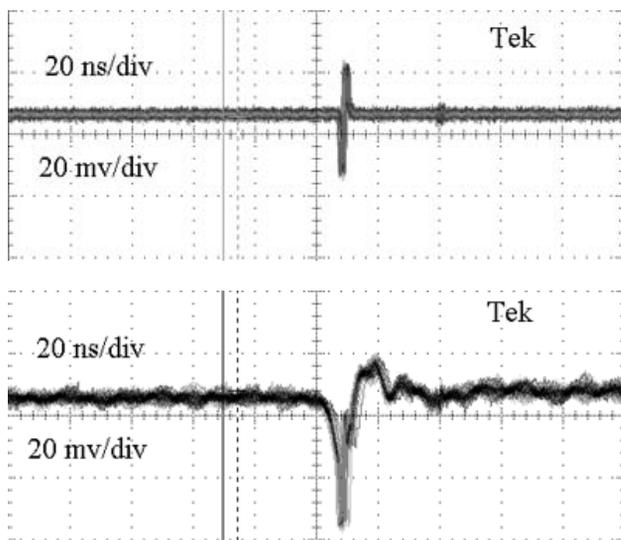

Figure 8: Single Bunch and Result of Delay Adjusting

Fig.8 shows the experiment result of delay adjusting. The upper plot of Fig.8 is the signal of single bunch from the upstream of stripline kicker, and the lower one is the result of delay adjusting. The square wave signal from upstream of stripline kicker, deriving from the DAC of the digital signal processor covered the single bunch signal, which meant the feedback signal was applied to exactly the same bunch.

Feedback effect

The transverse feedback system was commissioned in horizontal direction under 800MeV operation this May. Excitation effect of the transverse feedback system was observed during the experiment, while the beam spectrum and beam profile [5] with and without feedback are shown in Fig.9. When the feedback was turned on in horizontal direction, the frequency of horizontal tune was excited, and the beam profile enlarged in horizontal direction.
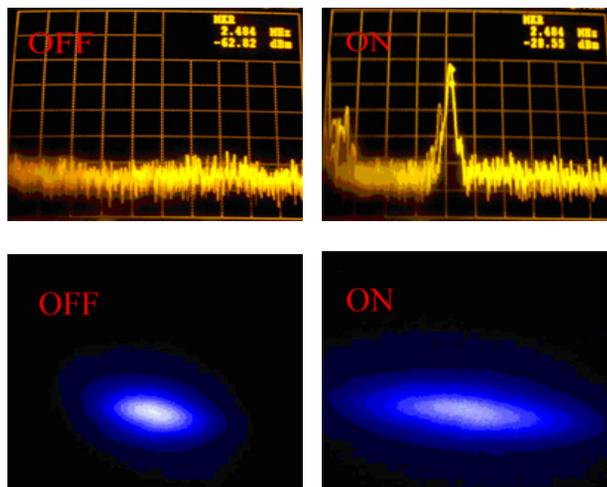

Figure 9: Spectrum and Beam Profile When Feedback OFF/ON.

To test the feedback system in vertical direction and to get the negative feedback effect are the next steps, which will be after August for there is no machine study time before September.

CONCLUSION

The digital transverse bunch-by-bunch feedback system was under developed in HLS. The primary experiment showed the positive feedback, and further investigation of the feedback system is needed to improve the performance of the system.

ACKNOWLEDGMENTS

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