A KICKER DRIVER FOR THE INTERNATIONAL LINEAR COLLIDER

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Abstract

Diversified Technologies, Inc. (DTI), under a SBIR grant from the U.S. Department of Energy, is developing a driver for a kicker strip-line deflector which inserts and extracts charge bunches to and from the electron and positron damping rings of the International Linear Collider. The ultimate ILC damping ring kicker driver must drive a 50 Ohm load (a 50 Ohm terminated TEM deflector blade) at 10 kV with 2 ns flat-topped pulses according to the ILC pulsing protocol, which is to burst pulses at a 3 MHz rate within one-millisecond bursts occurring at a 5 Hz rate. The driver must also effectively absorb high-order mode signals emerging from the deflector itself.

In this paper, DTI will describe a promising approach to the design of the kicker driver involving high voltage DSRDs (Drift Step Recovery Diodes) and high voltage MOSFETs. The prototypical system provides only 5 kV pulses, but otherwise satisfies the ILC requirements. Because of the very high pulse rate required, this design is using an all-electronic, rather than magnetic, approach to pulse compression.

BACKGROUND

Every particle accelerator requires "kickers" – electromagnetic deflectors that pulse on to divert (kick) bunches of particles out of their trajectory onto new beam paths targets, detectors, or other instrumentation. Kickers must operate very fast - typically in nanoseconds. They must reach their desired field between particle bunches, control that field for a finite time, and return to zero field before the next bunch arrives. The drivers for these kicker deflectors, therefore, must be capable of providing the required current into the kicker impedance on similar timescales.

The International Linear Collider (ILC) requires that bunches of electrons and positrons inserted into the main accelerator section of the ILC must be highly mono-energetic and well collimated. To achieve this, the use of "damping rings" is planned. A critical issue is that the ultimate size and cost of each damping ring strongly depends on the speed of the kickers. The challenge to the kicker electronics is enormous - bunch spacings must be slaved to the 650 MHz drive frequency of the linac itself. As a result, the shortest center-to-center spacing of bunches is 3.07 ns (occupying every other of two rf "buckets") and the next candidate spacing is 4.62 ns (occupying one of three rf "buckets"). The shorter of these is consistent with the smallest (6km circumference) ring described in the 2007 Reference Design Report. Construction of the ILC requires very fast kicker drivers to support these damping ring designs.

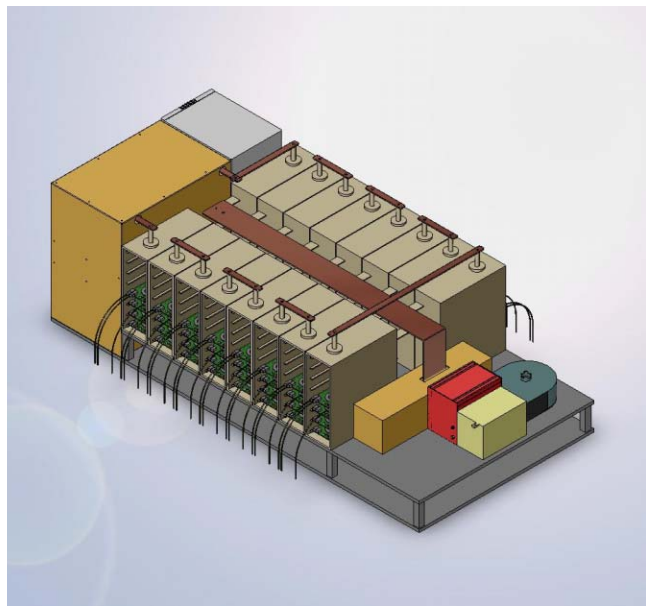

Figure 1: Proposed ILC damping ring pulse generator, approx. 36" long. Fiber-optic coupled controller not shown.

In Phase I of this SBIR, DTI addressed two related paths to meet the ILC kicker driver requirements for push-pull Transverse Electromagnetic (TEM) deflection for the ILC: a MOSFET ("pump") switch, and a Drift Step Recovery Diode (DSRD). Through this effort, we have demonstrated the underlying switching capabilities required to address the ILC kicker requirements, and move towards full-scale ILC class kicker drivers in Phase II (Figure 1).

OVERVIEWS OF THE TWO PROPOSED APPROACHES

The ultimate size, and hence cost, of each damping ring strongly depends on the speed of the kickers. The original (September 2005) SBIR solicitation for Phase I, in support of the ILC design, originally addressed rise and fall times of the deflection voltages, in the range of 3-20 ns, with a definite stated preference for 3-4 ns, in support of an 8 – 12 ns pulse duration**.** The speed parameter of interest to the accelerator community is termed "bunch spacing" which is the full duration of a pulse. During the period of the Phase I effort, these requirements tightened significantly.

The Snowmass ILC 2005 workshop proceedings stated that these rise and fall time durations relate to a rise to 98

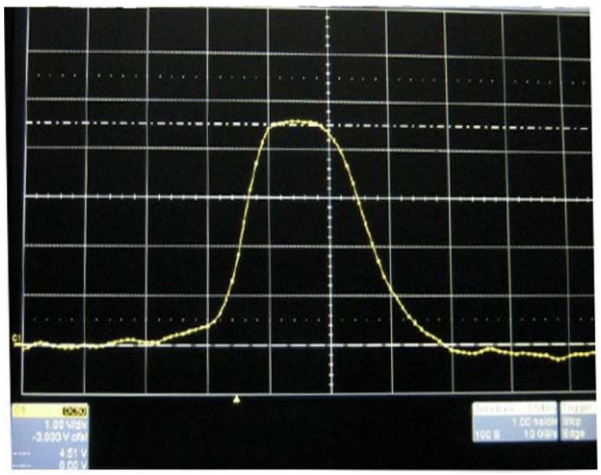

Figure 2: Pulse performance of table-top DSRD demonstrator (source: consultant Dr Anatoly Krasnykh). FWHM is 2 ns.

percent and a fall to 2 percent of flat-top voltage. Furthermore, the solicitation stated that the pulse rate must be 3 MHz for a burst duration of one millisecond, with a bursts repetition rate of 5 Hertz (i.e. the average PRF is 15,000 Hertz). Multiple kicker modules will be required to deflect the 5GeV beam by 0.6 mrads.

The essential objective of the project is to develop high-voltage, 2 ns pulses for deflecting packets of electrons and positrons from their respective damping rings (6 km circumference storage rings) into the 40-km long ILC linear collider, and for nearly simultaneous replenishing of the packets of charge in the damping rings. It is envisioned that an increment of deflection will be imparted by a symmetric pair of shaped parallel deflection blades of 30-cm length, pulsed in opposition at 10 kV each for two nanoseconds. (Ten stages of such deflection will be necessary to produce the overall "kick" required.) Within each guide comprised of the two 30-cm deflector blades and their environment, each TEM wave produced by the two pulse generators traverses from the entrance to the terminus of the guide in register with the selected (relativistic) charge packet. Matching 50-Ohm resistors terminate the deflector blades to avoid the creation of backward-traveling waves.

Various system designs were explored for producing desired pulse wave forms by exploiting the extremely abrupt opening of DSRD switches. Representative short pulse performance with the chosen pulse compression technology, drift step recovery diodes (DSRDs) is exhibited in Figure *2* The favored embodiment of the overall pulse generator was based on measurements, circuit modeling and practical considerations regarding component performance in the sub-nanosecond regime, is described below.

The overall pulse generation and compression network is presented in Figure 3. This represents the principal schema, but variants on this approach have been developed as well. The key components are exhibited in this figure including:

- A high voltage MOSFET switch array capable of delivering 25 ns, 400 A, 1 kV pulses at 3 MHz in one millisecond bursts, at a burst rate of 5 Hz; this switch array having a withstand capability of 4 kV or more.
- A DSRD diode stack initially capable of withstanding 5 kV upon opening (but later capable of 10 kV), able to open within 500 picoseconds, and interrupt 400 A reverse current.
- A one-nanosecond 50 Ohm delay line, together with an input circuit that presents a near-electrical-short to the line for frequencies greater than 10 MHz.

Not shown is a pulse output circuit that presents the TEM load with 50 Ohms immediately after the two nanosecond drive pulse has passed; this suppresses reflection of higher-order-modes excited within the deflector.

The presence of the delay line is essential. Its inductance ensures the input current pulse is maintained at

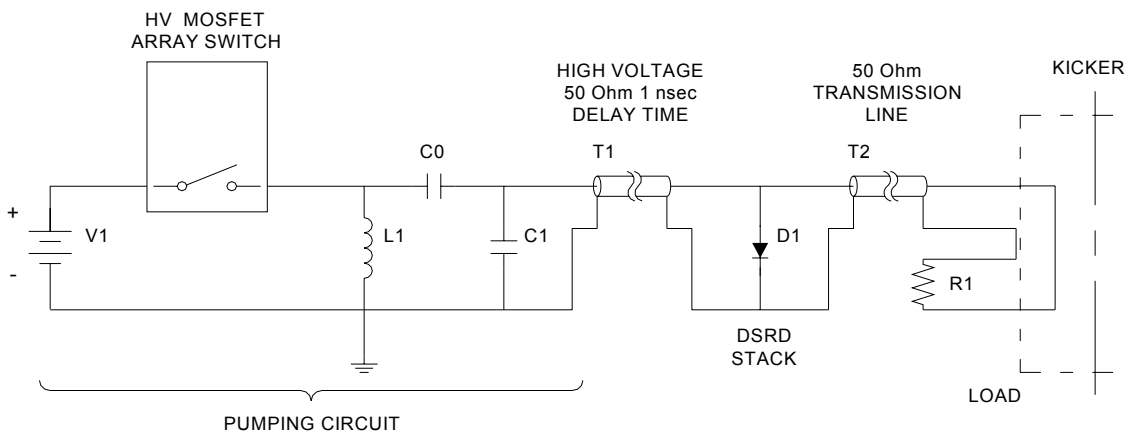

Figure 3: Basic pulse compression network employing a DSRD stack. Here V1 = 780V, L1 = 25 nH, C0=9 nF, C1 = 3F, ton = 25 ns.

the DSRD for a full two nanoseconds with little sag, and its high-frequency shorted input is expressed at the DSRD (and load) only after a round-trip of two nanoseconds, abruptly terminating the output pulse. Because this feed delay line is in parallel with the 50 Ohm load (actually a transmission line terminated by the 50 Ohm TEM deflector) the DSRD stack must interrupt 400 A to produce 10 kV pulses. We believe the use of such a delay line to feed the DSRD is unavoidable.

The operation of the overall network shown in Figure 3 proceeds as follows: the pump circuit to the left applies 780 V to the 25 nH transfer inductor for 25 ns. During and immediately after this brief pumping interval, a moderate forward current is established in the DSRD stack at the right, establishing narrow, highly concentrated minority carrier populations on both sides of the physical PN junctions within the DSRD diode stack. When the pump switch (the HV MOSFET array) opens, a large portion of the current that has been established in the transfer inductor must be suddenly drawn ***from*** the 1-nanosecond delay line, reversing the current in the conducting DSRD which, by design, opens extremely abruptly after a few nanoseconds delay (i.e. after the plasmas on both sides of the PN junctions collapse). The opening of the DSRD switch causes the reverse current of 400 A to redirect, splitting it equally between the 50 Ohm load and a reflection back into the 50 Ohm source line (i.e. the 1-ns delay line). This condition persists only for the 2-nanosecond round-trip in the delay line, after which the pumping source appears to the DSRD - and the load in parallel with it - as a short circuit, which terminates the 2 ns pulse impressed on the load. The predicted voltage across the MOSFET switch array and the load voltage are shown in Figure 44. Note in this case that delivery of a 10 kV pulse to the load requires that the MOSFET switch array must withstand a voltage of 3.5 kV after it opens.

SUMMARY

The DTI team has designed and demonstrated the key elements of a solid state kicker driver capable of meeting the ILC requirements, and extension to a wide range of kicker driver applications. The MOSFET array switch, without the DSRDs, is itself suitable for many accelerator systems with > 10 ns kicker requirements. Full scale development and test of this design are anticipated to occur in Phase II of this DOE SBIR effort, with a full scale demonstration in 2009.

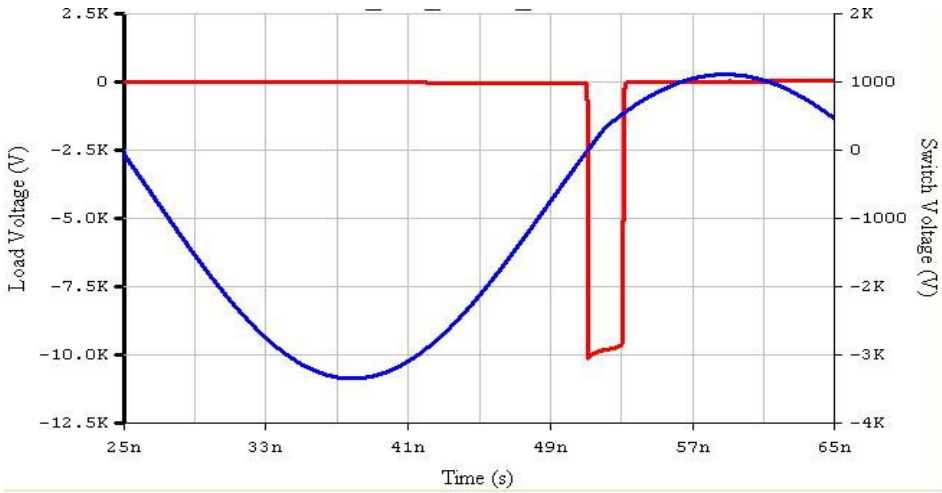

Figure 4: Predicted waveforms for the refined compression circuit which produces 10 kV pulses in a 50 Ohm load. Red curve (left axis) is the predicted load voltage, and the blue curve (right axis) is the voltage experienced by the pump switch (the MOSFET array). To produce a 10 kV output pulse the HV MOSFET must withstand 3.4 kV, although the gated voltage is only 780 V; note the voltage gated is only 780 V.