STATUS OF THE LOW-LEVEL RF SYSTEM AT KEK-STF*

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Abstract

RF field stabilities less than 0.3%, 0.3° are required at the STF low-level rf (LLRF) system. In order to satisfy these requirements, a digital FB system using an FPGA is adopted. A total of eight cavities will be installed in STF-phase 1 and the vector sum control of eight cavity signals will be achieved. The performance of the FB system is examined using electrical cavity simulators prior to the rf operation. Other R&D projects such as the development of a simplified interlock system with an FPGA are also summarized.

INTRODUCTION

The Superconducting RF Test Facility (STF) is the R&D facility of the International Linear Collider (ILC) [1]. In STF-phase 1, a cryomodule, which comprises four cavities with a 35 MV/m gradient and four cavities with a 45 MV/m gradient, and an rf (or dc) gun will be constructed. In STF-phase 2, three full-size (12 m) cryomodules will be constructed from FY2008 to FY2010 by employing the same unit as in the ILC basic configuration design (BCD). These superconducting rf cavities will be driven by a high-power klystron (1300 MHz, 1.5 ms, max. 5 MW or 10 MW, 5 Hz) and vector sum control will be applied to the cavity rf field.

The LLRF system of STF-phase 1 is based on the J-PARC linac [2] and the schematic is shown in Fig.1. The components are a programmable logic controller (PLC), touch panel (TP), digital feedback system using a compact PCI (cPCI), and fast interlock module; all these components are installed in two 19-inch standard racks. The PLC is used as the main system controller and ON/OFF commands are transmitted to the cPCI/FPGA and pulse modulator. The touch panel provides a GUI for local operation to access the PLC. The fast interlock module provides high-power protection by controlling the gate signal to the RF switch of the pulse modulator module in order to protect the high-power components such as the rf windows in case of rf discharge and rf overreflection.

DIGITAL FEEDBACK HARDWARE

The targeted rf stability is a value less than 0.3% in amplitude and less than 0.3° in phase. A digital feedback system is adopted for flexibility in the feedback (FB) and feedforward (FF) algorithm [Note: Please check the change.] implementation. The digital feedback system consists of an rf and clock generator (RF&CLK), mixers and I/Q modulators (Mixer/IQ-mod), an FPGA board, a DSP board, and an I/O board.

The RF&CLK unit generates an rf (1.3 GHz), LO (1.31 GHz), and two timing clocks (10 MHz, 40 MHz). The jitters calculated using the measured phase noise (from 100 Hz to 1 MHz) are 0.01° and 0.0083° for the LO and 40-MHz clock, respectively [3], which are sufficient to reduce the aperture jitter [4].

The Mixer/IQ-mod has ten active mixers (AD8343) and two IQ modulators (AD8349). A water-cooling system is adopted to stabilize the output signals of these RF&CLK and Mixer&IQmod units. The output signals of the mixer can be stabilized at a value that is of the order of 0.01° in phase by water cooling regulated within 0.1°C.

PERFORMANCE OF DIGITAL LLRF SYSTEM

The DACs on the FPGA board are connected to the IQ modulator. The rf output is amplified by a klystron and drive cavities. The rf probe signals from cavities are down-converted to an intermediate frequency (IF, 10 MHz). The IF signals are directly acquired by the ADCs and processed by the FPGA. The FPGA board has an

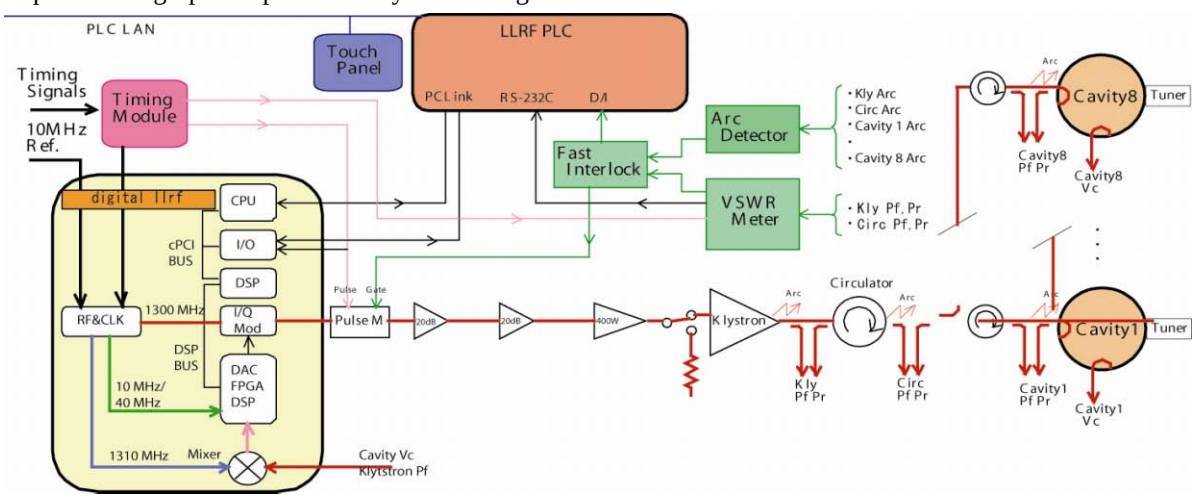

Figure 1: Schematic of the STF-LLRF system.

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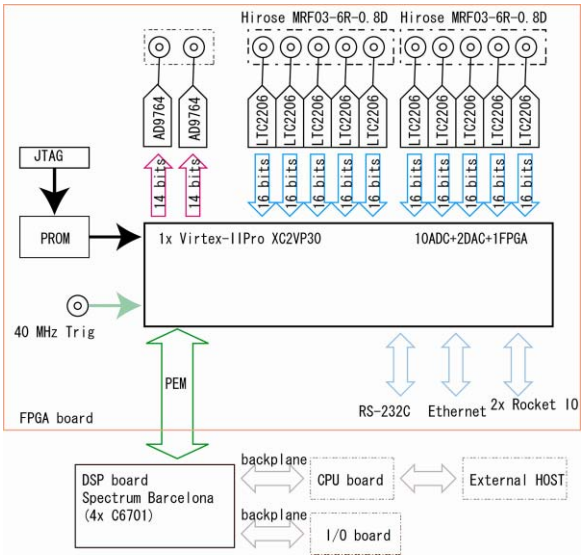

Figure 2: Schematic of the FPGA board.

FPGA (VirtexIIPro30), ten 16-bit ADCs (LTC2204), and two 14-bit DACs (AD9764); the FPGA board functions as a mezzanine card of a DSP board. The schematic of the FPGA board is shown in Fig.2. The input connectors of the IF signals are compact multichannel connectors (Hirose MRF03) in order to avoid the wrong connections and to save the front-panel area. Two fast serial ports (Rocket IO), an Ethernet port, and a serial port (RS-232C) are provided for future applications. Figure 3 shows the frequency spectrum for an input signal of 10 MHz (sampled with the 40-MHz clock for 4,000 points). Since no spurious signals are observed, further signal improvements will be possible by averaging the ADC signals.

A commercially available DSP board (Barcelona by Spectrum Signal Processing Inc.) is used for communication between the FPGA and the local host and will also be used for complex applications such as quench detection. Feedback parameters, set tables, and rf waveforms are transferred to the CPU board via the cPCI backplane.

In order to evaluate and develop a digital feedback system, electrical cavity simulators [5] are constructed

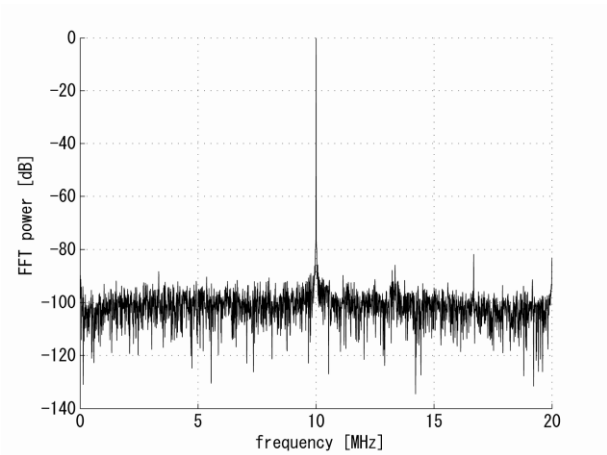

Figure 3: FFT spectrum obtained at 10 MHz input.

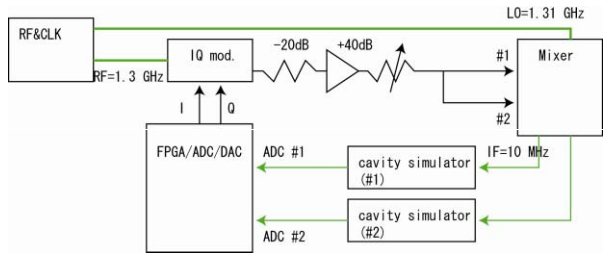

Figure 4: Performance test for the digital FB system.

using commercial FPGA boards (XtremeDSP by Xilinx). Both Lorenz force detuning and beam effects are included in the simulator. Four FPGA boards are installed in the PCI bus where the four cavity simulators run.

The performance of the feedback system was evaluated with these cavity simulators. IQ-modulated signals were down-converted to IF signals and these were provided to the cavity simulators, as shown in Fig.4. Vector sum control was carried out under PI control (without FF). Figure 5 shows the result at the set point of 28,000. The observed sag was caused by the FB with PI control. By using a proper FF table, such sag can be made to disappear. The corresponding noise in the amplitude and phase of the pulse was +/–0.05% and +/–0.03°, respectively.

LLRF MONITOR AND SERVER

The GUI program for the STF LLRF is built on a Common Object Request Broker Architecture (CORBA) platform. The CORBA client communicates with the DSP board through the cPCI bus, setting the LLRF parameters and tables. With the CORBA client, we can set the LLRF parameters and tables and input the waveforms of the ADCs and DACs. A Linux CORBA server stores the rf waveforms, i.e., the average and standard deviation waveforms during the rf flat top, every one minute. The stored data can be restored and analyzed by the CORBA client. The system layout is shown in Fig.6.

In the near future, we will install EPICS in cPCI and it will act as the EPICS IOC. Since a large amount of data such as those pertaining to cryogenic temperatures and the cavity status have been handled using EPICS, we can compare the LLRF data with the EPICS records.

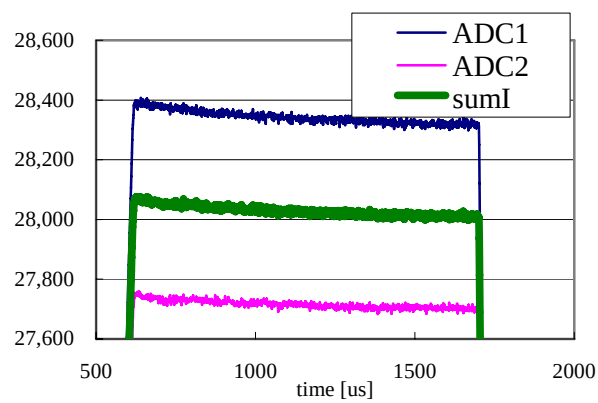

Figure 5: Vector sum control using cavity simulators.

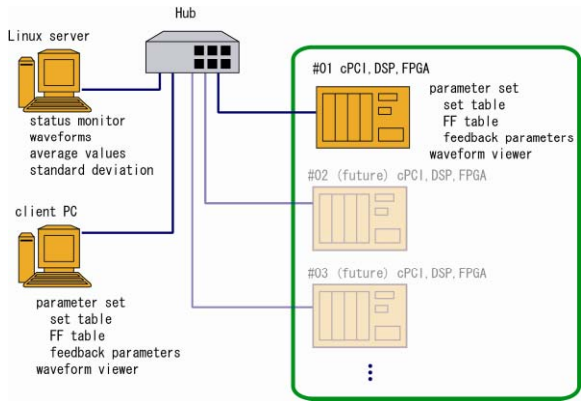

Figure 6: Schematic of LLRF data acquisition network.

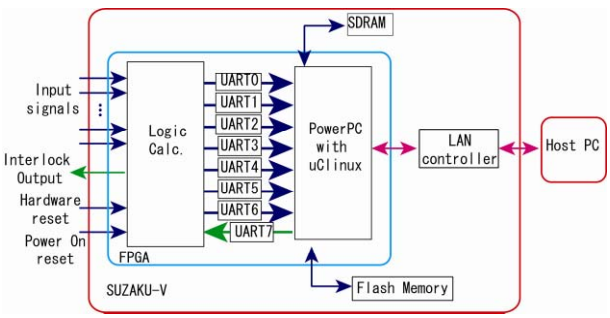

Figure 7: Interlock system using a Linux embedded FPGA.

LLRF R&D FOR ILC

Interlock System Using an FPGA Board

Instead of the present PLC interlock system, a simplified interlock system using a commercial Linux embedded FPGA (SUZAKU-V by Atmark Techno) is now being developed; in this system, the interlock logic is constructed by using an FPGA and the GUI is designed with Linux. The schematic of the FPGA interlock system is shown in Fig.7. In the FPGA chip, some simple logical calculations are carried out using the input signals to generate the interlock output. An embedded operating system called uClinux runs on the PowerPC core inside the FPGA chip. The status of the input signals is conveyed via seven universal asynchronous receiver transmitter (UART) serial ports to the uClinux system. The socket client has a GUI panel using which the operator can observe the interlock status or reset it. The reset command is sent through the eighth UART port.

Arc Detector

The conventional arc-detection method uses a photocoupler with a thick optical fiber. Instead of this, we adopt a compact photosensor module (H5784 by Hamamatsu Photonics) that has high sensitivity without requiring a high voltage supply. Owing to the high sensitivity of the photosensor, a cheap commercial optical fiber with a thinner diameter can be used. This system has been installed at the STF.

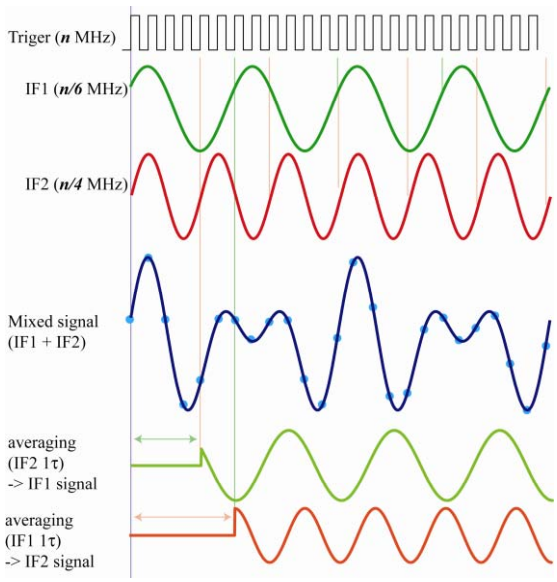

Figure 8: Concept of IF-mixture. By digital processing, two IF signals are restored.

IF-mixture

An IF mixture that can reduce the number of ADCs required for field detection is also under evaluation. The schematic of the IF mixture is shown in Fig.8. This example uses two IFs and the down-converted signals are mixed by a composer (IF1 + IF2). This signal is separated digitally (into IF1 and IF2) by using a proper filter. In the case of a two-IF system, we can reduce the number of ADCs by half. The principal examination has already been carried out [6].

SUMMARY

An LLRF system based on the J-PARC linac is constructed in STF-phase 1. An FPGA board having ten 16-bit ADCs and two 14-bit DACs is developed and the feedback performance with electrical cavity simulators satisfies the stability requirements. R&D projects for the ILC, such as the development of an interlock module and arc detection, are in progress. The IF mixture method that decreases the number of ADCs is also examined.

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