MULTICHANNEL VECTOR FIELD CONTROL MODULE FOR LLRF CONTROL OF SUPERCONDUCTING CAVITIES*

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Abstract

The field control of multiple superconducting RF cavities with a single Klystron, such as the proposed RF scheme for the ILC, requires high density (number of RF channels) signal processing hardware so that vector control may be implemented with minimum group delay. The MFC (Multichannel Field Control) module is a 33-channel, FPGA based down-conversion and signal processing board in a single VXI slot, with 4 channels of high speed DAC outputs. A 32-bit, 400MHz floating point DSP provides additional computational and control capability for calibration and implementation of more complex control algorithms. Multiple high speed serial transceivers on the front panel and the backplane bus allow a flexible architecture for inter-module real time data exchanges. An interface CPLD supports the VXI bus protocol for communication to a Slot0 CPU, with Ethernet connections for remote in system programming of the FPGA and DSP as well as data acquisition.

INTRODUCTION

The MFC board is an FPGA based 33 channel down-conversion and signal processing module designed for vector control of multiple cavities with a single Klystron such as the proposed RF scheme for the ILC[1]. An overview of the main components of the board is shown in Fig. 1. There are 4 DAC channels for RF outputs and multiple high speed serial transceivers on the front panel and the backplane bus to allow a flexible architecture for inter-module real time data exchanges. A floating point DSP provides additional computational capability for calibration and implementation of more complex control algorithms. Both the FPGA and DSP have external SDRAM memory for waveform and diagnostic data storage. Nonvolatile Flash memory is used for DSP program and FPGA configuration storage.

The interface CPLD supports the VXI bus protocol for communication to a Slot 0 CPU, with Ethernet connections for the control system interface, remote in system programming of the FPGA and DSP as well as for data acquisition and diagnostics.

SIGNAL I/O AND CLOCK DISTRIBUTION

Thirty channels of IF inputs are transformer coupled to 4 , 8-ch, 12-bit, 65 MHz ADCs with a voltage gain of 2, through an impedance matching filter network[2]. Two channels are DC coupled through differential ADC drivers with fixed gain. The 33'rd RF input is connected to a 14-bit, 105MHz parallel ADC through a transformer coupled impedance matching network. This channel can be used in a fast Klystron feedback loop to improve the cavity field vector control performance. An LO input of up to 1.6 GHz can be divided down to provide 8 clock signals through a clock distribution chip. The 4 8-channel ADC's and the clock distribution chip have digital calibration ports that are connected to the DSP's SPI bus which can be used for adjusting clock ratios, clock skew, generating test patterns and for powering down the ADC's between pulses. The digitized data from each ADC is transferred to the FPGA on 8 serial LVDS lines clocked at 6x times the sample rate with double data transfers in each clock period. Two dual channel 14-bit, 260 MHz DACs provide a total of 4 RF output channels. An optional auxillary clock input can be used to drive 2 DAC channels and two external trigger inputs are available to synchronize processing on the board. There are 8 additional backplane triggers that can be used for synchronizing clocks and other processes between boards.

SIGNAL PROCESSING FPGA

The primary signal processing functions of this board are performed in a Cyclone II FPGA (EP2C70F672C8). The device has 300 9-bit multipliers, 1.5 Mbits of Ram, 4 PLL's , 672 pins with 472 user I/O and 68000 LE with a max clock speed of over 400 MHz. Fig.2 shows the signal processing functions implemented in the FPGA.

Serial Data from the 32 RF channels is converted to 12 bit parallel in the Serial-Parallel latch. Downconversion is performed by multiplying the data with an 18 bit scaled and offset Cosine/Sine table to provide a composite gain plus rotation. The tables are 256 deep and they can be written to by the DSP or the slot0 CPU through the bus interface. The 24 I,Q pairs corresponding to the cavity fields are summed for vector processing. A pair of CIC filters completes the signal processing before the feedback error is computed. A gain and klystron linearizer multiplier table provides loop gain. A feedforward input is added and the output from the fast klystron loop is summed in before upconversion to the IF frequency. The I and Q signals are outputted to the external modulator through a dual channel 14-bit DAC. Reference signals for the beam and cavity phase (one for each cryomodule with 8 cavities each) are processed in 4 of the auxiliary channels. Phase computation is done in the DSP and the corresponding I and Q setpoint tables are updated. Extensive diagnostics are available at various points along the signal chain.

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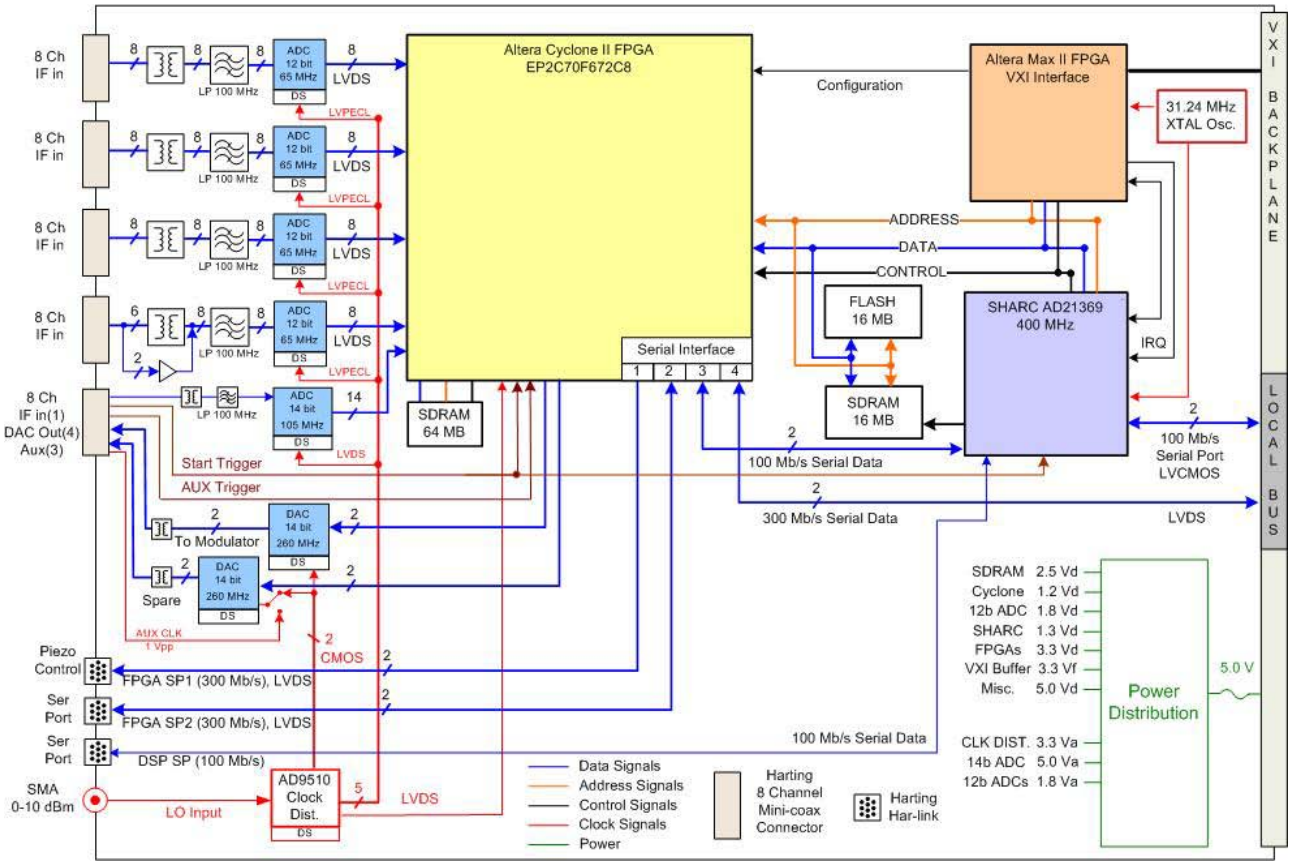

Figure 1: MFC Board Overview

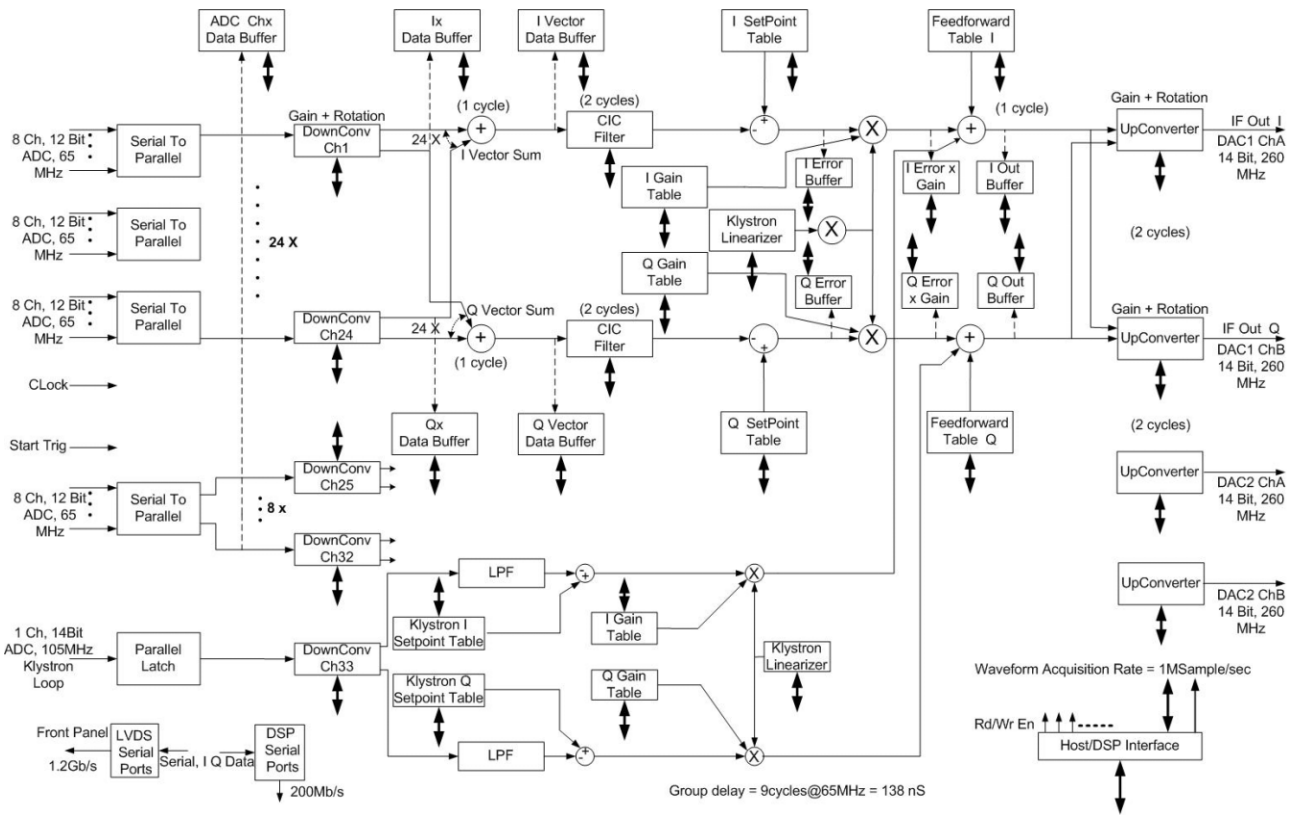

Figure2: FPGA Signal Processing

The tables and diagnostic buffers in the FPGA may be written to or read by the DSP or the slot0 CPU through the host and bus interfaces. Data can be transferred to the larger external memory through the SDRAM interface or may be read directly by the slot0 CPU.

TEST RESULTS

The results from testing of the prototype board are presented here. Figure 4 shows data acquired with the 1-channel 14-bit ADC. The measured noise floor is 110dB and it is close to the theoretical limit. The sampling frequency was 65 MHz and the input IF signal is 13MHz at 4 dBm power input.

Figure 5a shows the comparison between the FFT of one channel and the FFT of a vector sum of 6 channels. In the first case a signal with 10MHz IF frequency and +4dBm power is fed into the MFC board. Both graphs are displayed using the Hanning window. It can be calculated that the noise floor is approximately 70dB at bandwidth that equals half the sampling frequency. The red spectrum was obtained by feeding a signal with 13MHz IF frequency and +4dBm power into 6 channels. The spectrum represents the vector sum of these 6 channels. As can be seen there is a decrease of approximately 8dB in the noise floor. The sampling frequency in both cases equals to 1313MHz/21 and we acquired 16k of data.

Figure 5b shows the cross-talk between adjacent channels on the MFC board. For this test we fed a signal at 13MHz IF and +4dBm into one channel on the MFC board and observed the 13MHz component in adjacent channels. We acquired 16k of data at sampling frequency 1313/21MHz. According to the board layout (see board layout) the first figure represents measurements between two channels that are located on the top layer of the board. The second graph on the right is the same measurement but for three adjacent channels on the bottom layer of the MFC board. In all cases the signal was fed into the middle channel.

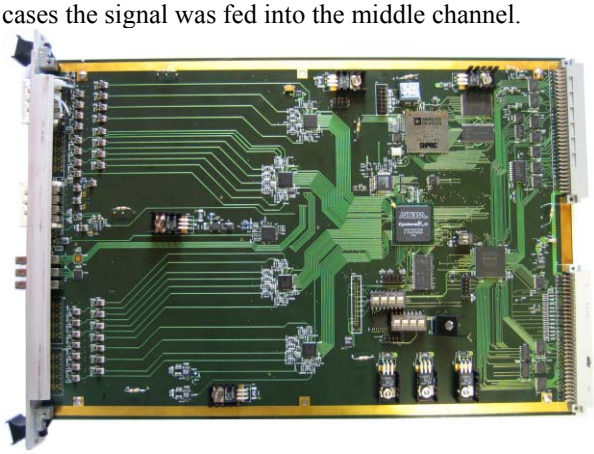

Figure 3: MFC board

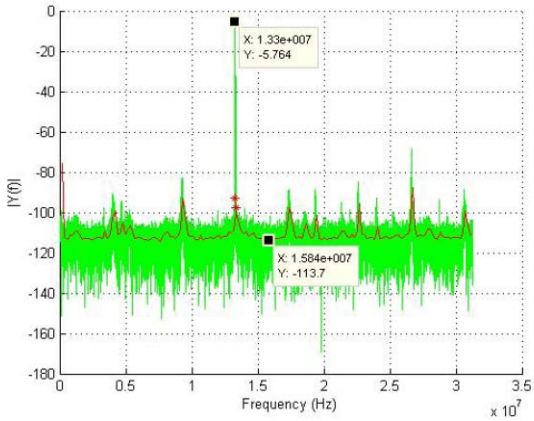

Figure 4: 14-bit ADC SNR

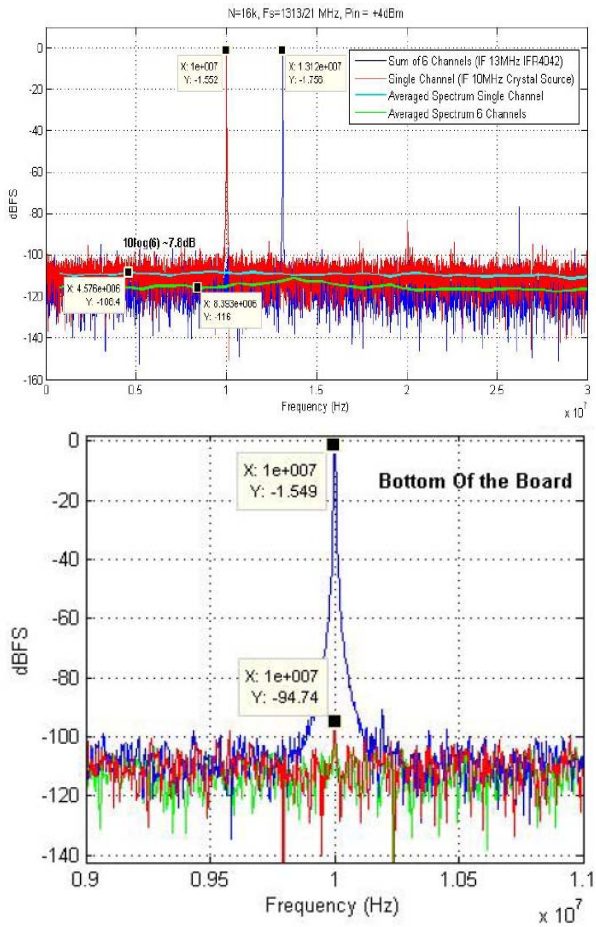

Figure 5: 8 ch ADC - Process gain and Crosstalk

REFERENCES

[1] J. Branlard, "Survey of LLRF Development for the ILC", PAC'07, Alburquerque, June 2007, FROA06.

[2] U. Mavric et al., "A 96 Channel Receiver for the ILCTA LLRF System at Fermilab", PAC'07, Alburquerque, June 2007, WEPMN102.

