PLANS FOR PRECISION RF CONTROLS FOR FERMI@ELETTRA

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Abstract

FERMI@ELETTRA is a 4th generation light source under construction at Sincrotrone Trieste. It will be operated as a seeded FEL driven by a warm S-band Linac presently serving as the injector for the ELETTRA storage ring. Operation as an FEL driver places much more stringent specifications on control of the amplitude and phase of the RF stations than in its present operation. This paper describes a conceptual design of new RF controls to achieve these specifications. The system consists of a stabilized distribution of the master oscillator signal providing a reference to local digital RF controllers. The RF controller is based on recent improvements on modern digital systems, using a 16-bit high speed digitizer in combination with an FPGA and high speed DAC.

INTRODUCTION

All-digital low level RF controllers for Linacs have become the standard over the past 5 years [1,2] with performance gains directly tied to industrial advancements in ADC, DAC, and FPGA technology. Growth in FPGA processing power has outpaced speed and accuracy improvements in the data converters and far outpaced improvements in noise and linearity of the analog RF elements. Consequently the burden of attaining higher performance for accelerator controllers will increasingly fall on the shoulders of the digital processor. The proposed low level RF control system for Fermi (FLLRF) will need to take full advantage of advancements in all areas in order to meet the required accuracy specification.

FERMI LINAC RF PARAMETERS

The Fermi Linac currently under construction at Elettra has an RF layout listed in Table1.

Table 1: Fermi Linac Parameters

RF Frequency	2998 MHz (S)		11992 MHz (X)
Klystrons	7	7	2
Cavity/Klystron	1	2	1

The maximum round trip klystron-cavity transmission delay will be 95ns in the single cavity configuration and 150ns in the dual. The total Linac length is about 150m.

Furthermore, the beam loading is negligible, the RF pulse width is 4μs and the rep-rate is 50Hz. The cavities are travelling wave structures with a filling time of 800ns to 1.4μs. The beam has a transit time of about 20ns, but sees the RF 'history' of the full filling time. Thus the necessary phase and amplitude stability of the RF field is specified as the rms value integrated over the fill time. This jitter should not exceed 0.1º and 0.1% on a pulse to pulse basis.

Two reference signals will be distributed to each LLRF system. The first will be a phase reference distributed in fiber with active phase control. The stability specification for this reference will be 0.03º and 0.04º for the S and X-band frequencies respectively. The second distributed signal will be a frequency reference of 483 MHz used to create various IF, LO, and sampling frequencies in both the S and X-band control systems. The required phase stability for this signal is considerably more lax since all measurements will be made in relation to the phase reference. Fig. 1 shows the various internal frequencies for both the S and X-band systems and the scheme by which they are created from the frequency reference.

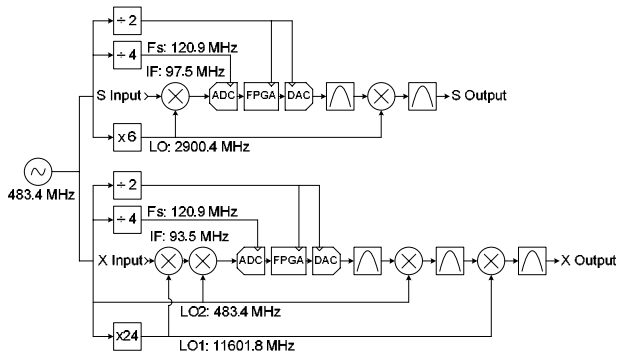

Figure 1: Frequency generation scheme for IF, LO and Fs.

FERMI LLRF ARCHITECTURE

System Configuration

Fig. 2 shows the configuration for the Fermi low level control system in a single cavity per klystron arrangement, while Fig. 3 shows the proposed system architecture for the S-band sections.

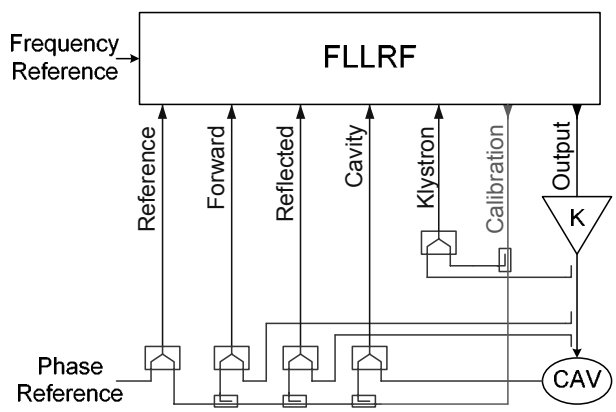

Figure 2: Fermi LLRF control system configuration.

Each system will have 5 identical high speed, high resolution, input channels and 2 identical high speed, high

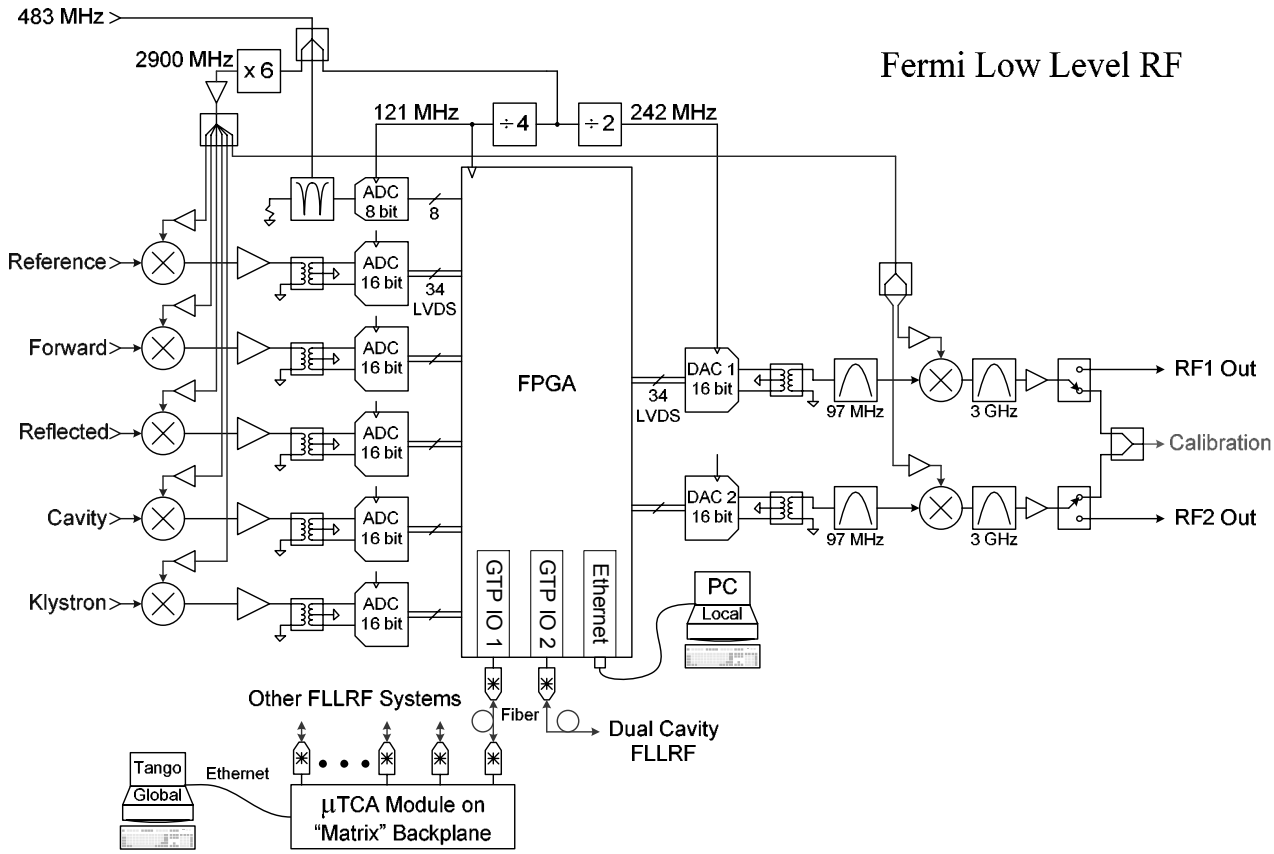

Figure 3: Fermi LLRF control system architecture for S-band section.

resolution output channels. The output channels can be configured to drive separate outputs or combined into a single drive.

ADC/DAC Requirements

The total RF pulse to pulse stability budget of 0.1º and 0.1% requires that the measurement be at least a factor of three better. This corresponds to a minimum resolution of 12.6 bits for bi-polar operation. Averaging will likely be needed to achieve this goal with either 14 or 16-bit ADCs. A high data rate and low aperture jitter are also important since the IF signal will need to be 50 MHz or higher in order to make the output filter realizable. LVDS outputs would be useful to reduce digital switching noise. Finally, a direct feedback loop around the klystron is foreseen making low latency a desirable feature. The LTC2208, which offers 16-bit LVDS outputs at up to 130 Msps with 70 fs jitter and 7 cycle delay, is foreseen to be used as the ADC. The requirements on the output DAC are less critical however a data rate twice that of the ADC, 16-bit resolution, and LVDS outputs are desirable. The AD9726 meets these demands.

IF Frequency and Non-IQ Sampling

Non-IQ sampling offers the combined benefits of providing a method to average out the integral nonlinearity (INL) of the ADC while simultaneously placing any IF harmonics away from the carrier [3]. The cost is a more complex processing algorithm. The choice of 483 MHz as the reference frequency leads to a sampling rate of 121 Msps and an IF of 97 MHz. This places the IF in the second Nyquist zone which will alias the signal (with a frequency reversal) to 23 MHz. The troublesome 2nd, 3rd, and 5th harmonics are well separated from the fundamental. The lowest even harmonic to alias near the fundamental is the 4th, and the lowest odd harmonic to do so is the 9th. The IF is sampled every 290.3º so that 31 values of the ADC's output code are used (as opposed to 4 for normal IQ sampling). The averaging of these will help reduce the effect of the ADC's INL (±1.2 bits for the LTC2208).

Calibration and Correction

At high RF frequencies it becomes increasingly difficult to maintain constant phase length in the input lines. For example even with phase stabilized cable (LDF2-50, τ_{cd}: 5.6 ppm/ºC) a 1ºC change in temperature in 1 meter of cable will absorb a quarter of the overall S-band phase budget. A scheme has been developed, illustrated in Fig. 2, to measure the phase drift in the input lines and compensate for it with digital processing [4,5]. Between pulses a calibration signal is sent through the input lines. The phase drift in the cables can be deduced from the measurement. The sections highlighted in red can not be compensated for and must be short or in a temperature controlled environment.

Third-order distortion products from active elements in the input chain, primarily the mixer, will contribute to

uncorrectable errors. However, if this distortion can be characterized the errors can again be compensated for with digital processing. Having two independent output channels allows the system to send a pure two-tone signal through the calibration line allowing the intermodulation products of the input channels to be measured.

Machine Timing

A fiducial sync signal will be sent to all systems along the 483 MHz frequency reference line in the form of a frequency bounded sinc waveform which can be extracted with a diplexer. A high speed 8-bit ADC will be used to detect the sync signal from which a temporal resolution in the 10's of picoseconds can be extracted. A periodic series of these pulses, referenced to the high stability phase input, has the potential for several uses:

- The transmission of machine timing events.
- The transmission of a fiducial used to simultaneously align the various frequency dividers at all stations.
- The precise transmission of TAI/UTC time.
- Power-on reset synchronization.
- Integrity check of all FPGA counters and clocks.

Control Algorithm

The low level system will be able to support a variety of control loop structures. A direct feedback loop around the klystron with a bandwidth on the order of 1 MHz should be feasible due to the short transport delays and relatively low processing latency. This loop will help to isolate the cavity phase from voltage droop on the klystron during the 4μs pulse.

The primary control however will use feed forward on a pulse to pulse basis. The system will acquire data during the pulse and have ample time (20ms) to formulate the drive for the next cycle. Naturally, this system will not be able to respond to random or nonrepetitive errors which hence must otherwise be maintained well below the field stability criteria. However, repetitive errors, even with relatively high bandwidth, can be controlled with the memory requirements of the system being proportional to the repetition period of the errors. Due to the short pulse length the memory requirements should not exceed the capabilities of modern FPGAs. For example the smallest DSP oriented FPGA in the Xilinx Virtex 5 family has sufficient on-board RAM to store the raw data from 68 pulses (4μs sampled at 121 Msps) on 5 channels.

SYSTEM COMMUNICATION

Local Communication

Unlike many low level control systems currently in use, the FLLRF will not be based on any backplane communication and power standard (VME, VXI, etc). Instead the FPGA will have three full-duplex serial communication ports configured as follows:

- An Ethernet port used for local control when debugging or testing.
- A high speed (3.2 Gbps) GTP link, over fiber, used to connect control systems together.
- A high speed (3.2 Gbps) GTP link, over fiber, used to connect each system to a central controller.

The GTP links on each controller can be daisy chained to connect several systems when more that 5 inputs are needed (for instance in the two cavities per klystron configuration). The speed of the links (16 bits @ 200 MHz) should add only minimal delay to the processing. The system will be enclosed in a standard 19" chassis containing the necessary power supplies and cooling.

Global Communication and 'The Matrix'

The communication link between each controller and the global control system (Tango) will be done through a MicroTCA standard module and backplane known as 'The Matrix' being developed at CERN. The module, which has 16 GTP fiber connections (sufficient for the complete Linac), connects to the backplane which has an Ethernet connection over which it can communicate to conventional server and/or workstation hardware. The module has 20 GTP links to the backplane, a 72x72 crosspoint switch capable of 3.2 Gbps and a V5 LX110T FPGA. The backplane has two 3.2 Gbps 144x144 crosspoint switches connecting the module links. This incredible connectivity opens the door for high bandwidth time deterministic communication between LLRF controllers or other diagnostics connected to a separate module on the backplane.

CONCLUSION

The first working prototype of the FLLRF system should be available in 12 to 18 months.

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