IMPROVED TUNING METHODS FOR CONVERTER-MODULATORS*

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Abstract

The converter-modulator is a resonant power conditioning configuration that is optimized for a particular load impedance or parameter space. Although traction motor Insulated Gate Bipolar Transistors (IGBT's) are typically used for hard-switching application in the 1 kHz regime, the present use of high-power (10 - 15 MW) converter-modulators have used a 20 kHz resonant switching topology. This presents design challenges to maintain efficient and reliable switching characteristics for the IGBT's. Improved tuning methods and circuit topological changes now offer a significant reduction in IGBT switching losses as compared to those used on the Spallation Neutron Source (SNS) design (perhaps by 10). These circuit and topology changes should also permit Pulse Width Modulation (PWM) of the modulator output voltage to provide a regulated voltage without anomalous IGBT switching characteristics. This paper will review the results of this investigation based on models developed from the SNS converter-modulator operational data.

INTRODUCTION

Los Alamos National Laboratory (LANL) has been examining improved converter-modulator design topologies to enhance many operational performance parameters. These parameters include flat-top regulation with PWM [1], reduced IGBT switching losses, reduced IGBT free-wheeling diode losses, increased overall efficiency, and improvements related to IGBT operational voltage and induced switching dV/dT. These design changes will significantly improve the reliability area of concern, those related to the IGBT's. The reduced operational voltage improves the IGBT Failure In Time (FIT) rate [1], a lifetime factor determined by the link voltage and duty cycle for an "H-bridge" configuration. The design improvements also significantly reduce switching dV/dT that improves the IGBT susceptibility to latch-up failure. As a starting point for this next generation converter-modulator, we used the IGBT performance data that we measured from the SNS operations and the same overall converter-modulator topology. As a direct comparison with same duty cycle and load parameters, we then modified the SNS circuit configuration and then using adaptive algorithms in the computer program to provide a flat-top pulse and determined the resulting changes as related to the above mentioned parameters.

EXISTING DESIGN TOPOLOGY

The existing designs do not utilize feedback of the output pulse to maintain a flat top (via PWM) because of concerns related to the IGBT's. This ensures fixed IGBT switching parameters through-out the pulse. This droop, as typical of existing systems, can be noted in Figure 1.
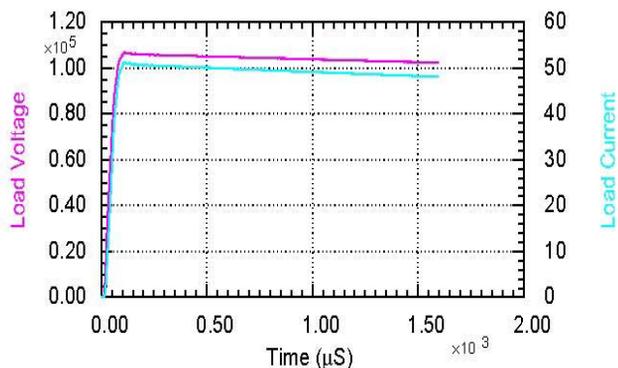

Figure 1: Unregulated Converter-Modulator Droop.

For this modelling, we used the same SNS converter-modulator design topology with circuit improvements to reduce IGBT commutation current, similar to that recently utilized for the Stanford International Linear Collider (ILC) L-Band Test Stand [2]. This reduces IGBT switching losses from the initial SNS design, but the overall IGBT switching loss remains somewhat high, about 2.3 kW per device. This power loss is for a 60 Hz repetition rate and 1.5 mS pulse (9% duty). The IGBT device package rating is ~16 kW but to minimize thermal cycling failures, IGBT losses should be kept below ~4 kW. The plot in Figure 2 shows the individual IGBT switching losses for this tuning method, ~38 Joules per IGBT, during each 1.5 mS pulse.
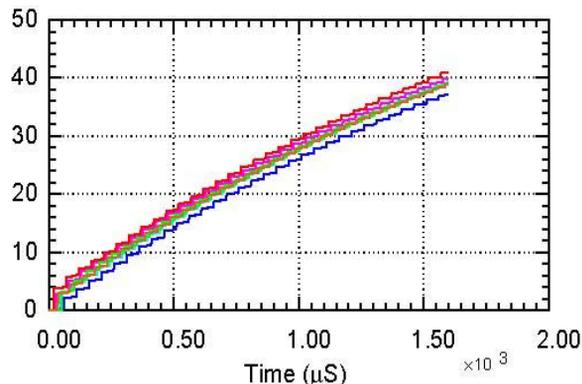

Figure 2: IGBT Switching Losses (Joules).

The reduced IGBT commutation current tuning method also reduces the DC buss link voltage from the SNS design of 2.4 kV to about 1.9 kV. This has a positive affect on the IGBT FIT voltage de-rating factors as well as the voltage margins for the SCR's used in the capacitor bank buss-link pre-regulators. Unfortunately, for a given capacitance, the effective stored energy is reduced. The overall droop of the capacitor bank is then about 4.5%, as shown in Figure 3.
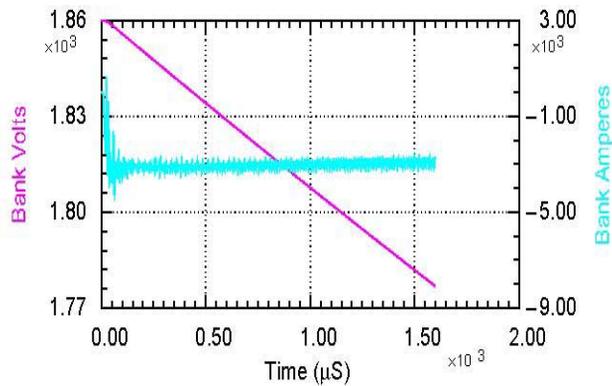
Figure 3: Link-Voltage Droop (~4.5%).

The present converter-modulator topology switches very quickly with over 9 kA per uS dI/dT and over 4 kV per uS dV/dT. These fast switching parameters although ideal from a switching loss stand point, are not necessarily desirable in regard to harmonic currents, induced feedback (e.g. Miller feedback to the IGBT gates that can cause spurious turn-on), and other anomalous parasitics such as inductive kick-back and skin-depth related losses. The plot in Figure 4 shows the collector-emitter voltage waveforms of the totem-pole connected IGBT's.
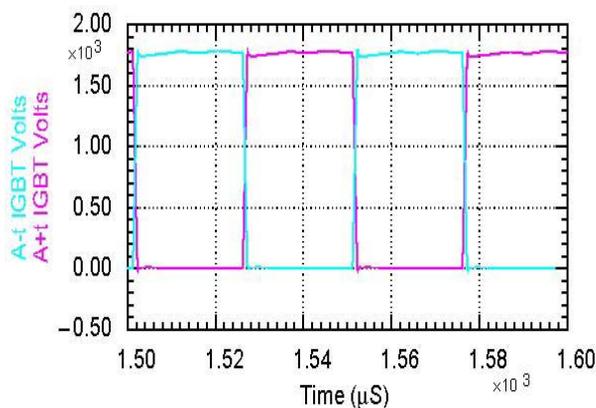
Figure 4: Totem-Pole Pair IGBT Collector-Emitter Voltages.

IMPROVED DESIGN TOPOLOGY

With simple changes to the converter-modulator topology coupled with changes in the tuning optimization, significant improvement in the overall performance and efficiency can be attained. In addition, these changes will reduce the dynamic and thermal stresses of the IGBT's and buss link components (e.g. bypass capacitors). Figure 5 shows the flat-topped output waveform with a regulation of about .25% and no turn-on overshoot. This is for that same case with ~4.5% bank voltage droop. We have also modelled a similar result with a bank voltage droop of 10%. We have yet to obtain good result with bank droops approaching 20%.
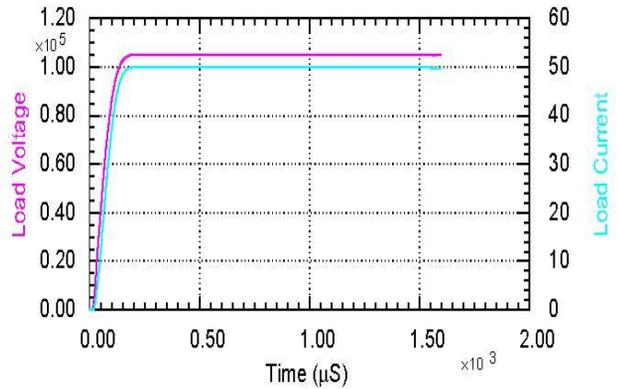
Figure 5: Flat-Topped Output (~.25%) with PWM.

An interesting result of this improved tuning method is that the IGBT switching losses are reduced by a factor of almost 6. The IGBT switching losses went from 38 Joules per pulse to about 6.5 Joules per pulse. This, no doubt, reduces thermal cycling as well as the average power loss, from 2.4 kW per device to less than 400 W per device. With less than 400 W dissipation per device, perhaps one could consider air cooling of the IGBT's. This would remove all water and plumbing circuits from the "safety enclosure", the enclose that contain the IGBT switch plate assemblies and capacitor energy store.
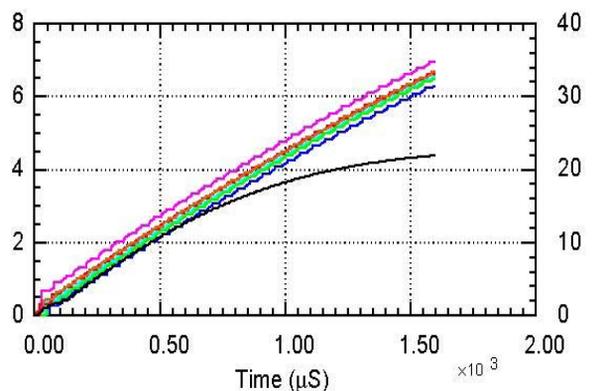
Figure 6: IGBT Switching Loss (Joules), Improved Tuning.

Another significant improvement is that related to the IGBT induced dV/dT. This reduced dV/dT reduces the Miller feedback voltage that appears on the gate of the IGBT's. Because of the fast switching, elevated values of gate drive are required to ensure appropriate switching and cut-off. With reduced values of dV/dT, lower gate drive voltages can be used that also minimize fault current

and extend the required IGBT recovery time before failure or latch-up. The reduced dV/dT also directly reduces the probability of latch-up. The slower dV/dT reduces the harmonic content of the switching waveforms and IGBT bypass capacitors, reducing their temperature rise. Although manufacturers do not typically specify gate power ratings of the IGBT's , but perhaps it is in the range of 20 W, the lower dV/dT should reduce that loss also. Depicted in Figure 7 are the collector-emitter voltage waveforms of the totem-pole connected IGBT's, with significantly reduced (by 6) the switching dV/dT. This reduction is a result of changes in the circuit topology and overall tuning methodology.
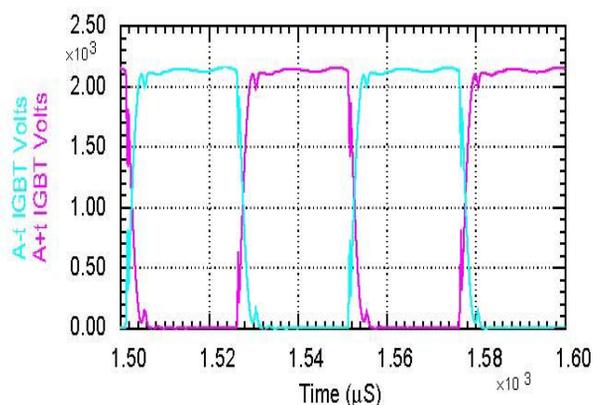

Figure 7: Improved Tuning Collector-Emitter Voltage.

CONCLUSION

The improved tuning methods and changed circuit topology will be used on the next generation converter-modulator designs. These improvements should enable the viability of adaptive feedforward and feedback techniques for the PWM circuitry that provide flat-top pulses. This permits a reduction of the stored energy. In addition, improvements to the overall system efficiency will result, to perhaps better than 95%. The tuning methods and circuit topology changes significantly reduce IGBT power loss and dynamic stresses, improving their reliability. Other desirable results are realized due to reductions in the harmonic content of the switching waveforms that tend to induce spurious responses. We look forward to detailing these successful results in the near future.

REFERENCES

[1] W. A. Reass et al., "High-Frequency Multimegawatt Polyphase Resonant Power Conditioning", IEEE Transactions Special Issue on Power Modulators and Repetitive Pulse Power, Vol.33, No. 4, August 2005, pp 1210-1219. (ISSN0093-3813).

[2] W. A. Reass et al., "Converter-Modulator Design and Operations for the "ILC" L-Band Test Stand", PAC07, Albuquerque, NM.