DYNAMIC FAULT DETECTION CHASSIS FOR THE 1MW HIGH VOLTAGE CONVERTER MODULATOR SYSTEM AT THE SPALLATION NEUTRON SOURCE*

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Abstract

The high frequency switching megawatt-class High Voltage Converter Modulator (HVCM) developed by Los Alamos National Laboratory for the Oak Ridge National Laboratory's Spallation Neutron Source (SNS) is now in operation. One of the major problems with the modulator systems is shoot-thru conditions that can occur in an IGBT H-bridge topology resulting in large fault currents and device failure in a few microseconds. The Dynamic Fault Detection Chassis (DFDC) is a fault monitoring system. It monitors transformer flux saturation using a window comparator and dV/dt events on the cathode voltage caused by any abnormality such as capacitor breakdown, transformer primary turns shorts, or dielectric breakdown between the transformer primary and secondary. If faults are detected, the DFDC will inhibit the IGBT gate drives and shut the system down, significantly reducing the possibility of a shoot-thru condition or other equipment damaging events. In this paper, we will present system integration considerations, performance characteristics of the DFDC, and discuss its ability to significantly reduce costly down time for the entire facility.

INTRODUCTION

The HVCM is capable of delivering pulses up to 11MW peak, 1MW average power at voltages up to 140kV to drive klystrons rated up to 5MW, at a duty cycle of up to 8%.The reliability of the HVCM is a key piece to the overall availability of the liner accelerator, and has typically run in the thousands of hours during initial accelerator operations. The goal for the modulator system, borne out of MIL-HDBK-21F calculations is 25,000 hours mean time between failures (MTBF). The goal for the entire SNS facility is 95% availability by FY2011 [1]. If 50 major subsystems are identified, an individual subsystem availability of 99% would be required to meet this goal. Present modulator statistics of 99.7% availability fall short of the goal, but demonstrating the calculated reliability will achieve the desired goal.

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Minimizing HVCM failures and early failure precursor detection have been under development since the initial HVCM instillation at SNS. As of early 2007, the total number of modulator failures has been approximately 17, with half of those attributable to IGBT failures caused by either transformer saturation, shoot-thru faults, or thermal cycling of the discrete junction [2]. The DFDC designed at Los Alamos National Laboratory, was installed on the modulator system to mitigate the transformer saturation-induced failures as well as those attributable to rapid voltage change during the flattop portion of the output waveform caused by HV component failures.

SYSTEM INTEGRATION

The DFDC is integrated with an Allen-Bradley programmable logic controller (PLC), a Control Chassis, and a SCR Control Chassis, as shown in Figure 1. The DFDC output is directly wired to the (PLC) controller which is interfaced to a Panel View 1000 color terminal display; this output provides status bits and displays it on the panel view. All modulator faults are detected and latched in the PLC or Personnel Protect Chassis and require a reset to clear, locally for personnel protection faults or via EPICS or the Panel View interface for equipment protection faults. The PLC performs the following functions, hardware I/O interfacing and data logging, local operation (Man Machine Interface), network interfacing for remote operation, fault detection and handling, operational state machine, and voltage control algorithm. The Fiber optic output of the DFDC is connected directly to the input of the Control Chassis; this output sends a command to the Control Chassis to disable IGBT gate drives. The control chassis generates IGBT timing signals from the master gate, implements fast data acquisition hardware with latching capabilities and provides the electronics to detect and respond to fault conditions requiring a timely response such as over voltage faults, over current faults, run permit faults, timing faults, and hardware faults. The SCR output of the DFDC is wired to the input of the SCR Control Chassis; this output sends a command to the SCR Controller to inhibit all SCR inputs, and closes the dump relays. The SCR is a +/- 1300 Volt DC freestanding 6 pulse power supply.

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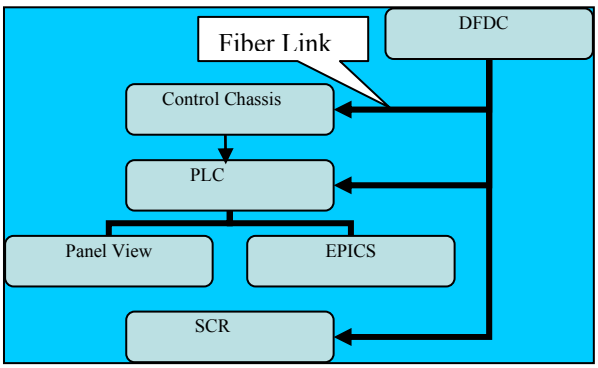

Figure 1: System Block Diagram

The SCR controller utilizes a self contained PLC, an Allen-Bradley Micrologix 1000, for error, state control and interlock processing. When the DFDC detects a fault, a fault interrupt command is sent to the Control Chassis, the Control chassis disables all IGBT gate drives forcing the modulator to shutdown as shown in figure 1 and sends a inhibit command to the SCR Control Chassis to inhibit the power supply, which closes the dump relays to discharge the capacitor bank. The Control chassis also sends status to the PLC. The PLC will enter the standby status, and as a result of the fault a reset is required to clear the fault before a transition back to the run state is allowed.

DESIGN

The boost transformer dB/dt signals are tapped off from a single turn on the core of the transformers and are used as DFDC flux inputs as shown in figure 2. The flux inputs go through a RC integrator stage, a differential amplifier stage, and finally a window comparator. If the flux level exceeds the comparator's reference voltage, the comparator's output will change states, (transition from high to low). The output of the comparator is then sent through a series of inverters, logic gates, latches and drivers that show indication on the front panel and the PanelView and EPICS screens that a fault occurred. The Dynamic Fault uses the same window comparator scheme. The gate input goes through a driver stage, and finally a logic stage to generate a strobe pulse with a delayed rising edge to eliminate spurious trips during the risetime portion of the modulator output voltage. The modulator output voltage waveform is differentiated through an amplifier circuit, with adjustable sensitivity, and compared to the raw modulator output voltage during the strobe period created with the delayed pulse. If a dV/dt event occurs during the strobe period, a fault is generated which truncates the gate output from the control chassis and passes through a series of inverters, logic gates, latches and drivers showing indication on the front panel that a fault occurred. Additional comparator circuitry is used to monitor the modulator voltage during the interpulse period and generates a similar response if voltage is detected outside the expected gate pulse. A few design modifications were needed to improve the reliability of the DFDC. The flux output was riding on a DC offset requiring us to set the comparator threshold values above levels where saturation would have been detected. To alleviate this problem, a high pass filter was placed in series with the window comparator's input to eliminate the DC offset. Additionally, a RC circuit was added to the strobe pulse to increased dynamic range in the strobe pulse delay.

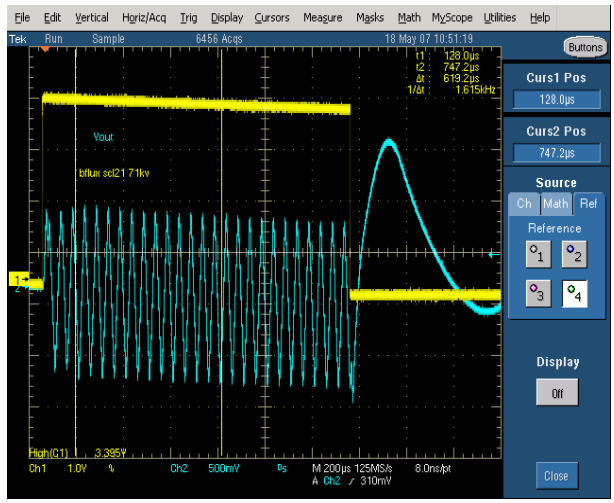

Figure 2: Transformer Flux

SYSTEM RESPONSE

The DFDC monitors the status of the modulator. When faults are detected, the DFDC sends commands to the Control Chassis, the PLC, and the SCR Control Chassis as shown in Figure 1. The fastest response resulting in system shut down is the fast fault out of the DFDC which is fiber-linked to the control chassis. Since the intent of the DFDC is to disable IGBT firing if an event is detected, this implementation represents the fastest mechanism to prevent energy transfer to the possibly failed components. The measured system response time is 1.26µs as shown in Figure 3.

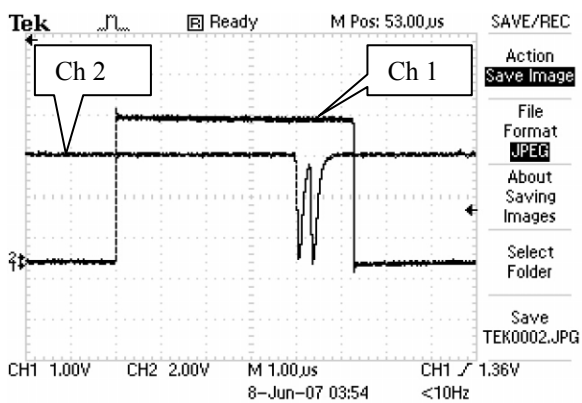

Figure 3: System Fault Response Time

Channel 1 displays one of the six IGBT timing signals. Channel 2 represents the shutdown pulse of the DFDC. The modulator is brought to the RUN state and 4.0μs later a DFDC fault is forced, sending a command via fiber to the Control Chassis. The Control Chassis receives the command and proceeds to shut the modulator down, terminating the IGBT gate signals as indicated in Figure 2. The whole sequence of events from the falling edge of Ch2 (DFDC detects fault) to the falling edge of Ch1 (Control Chassis response to DFDC command) takes 1.26μs. Several tests were conducted and the system response time varied from 1.08μs to 1.38μs, which is an overall average of 1.26μs.

CONCLUSION

To date, 15 DFDC's have been installed and integrated with the existing HVCM systems. System Mean Time Between Failures (MTBF) during CY2007 through late-March have improved to approximately 11,000 hours, partially as a result of installation of the DFDC system and responding to imminent problems. None of the failures during that period were directly attributable to the subsystems the DFDC was designed to protect. Additional activities planned for the DFDC system include refining the setpoints and investigating improving the noise immunity.

REFERENCES

[1] G. Dodson, private conversation, June 2007.

[2] D.E. Anderson, J. Hicks, M. Wezensky, D. Baca, and W. Reass, "Operational Performance of the Spallation Neutron Source High Voltage Converter Modulator and System Enhancements", *Proc. 27th IEEE Power Modulator Symposium*, Washington, D.C., 2006, p. 427.

