A SIMPLIFIED APPROACH TO ANALYZE AND MODEL INDUCTIVE VOLTAGE ADDER *

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Abstract

We have recently developed a simplified model and a set of simple formulas for inductive voltage adder design. This model reveals the relationship of output waveform parameters and hardware designs. A computer simulation has demonstrated that parameter estimation based on this approach is accurate as compared to an actual circuit. This approach can be used in early stages of project development to assist feasibility study, geometry selection in engineering design, and parameter selection of critical components. In this paper, we give the deduction of a simplified model. Among the estimation formulas we present are those for pulse rise time, system impedance, and number of stages. Examples are used to illustrate the advantage of this approach. This approach is also applicable to induction LINAC design.

INTRODUCTION

In our earlier papers [1] and [2] , we presented an inductive voltage adder (IVA) transmission network model based on circuit element simplification approach and a set of estimation formulas derived from the model. It was the first step to reveal IVA mechanism. They are intended for industrial applications.

We introduce here an expanded model and a more formal approach of IVA analysis.

SIMPLIFICATION

A single cell circuit model of inductive voltage adder was given in [3] and [4]. However, this single cell model is unsymmetrical. We change this model to a symmetrical one as in Figure 1. Where, SW is the main switch, C_S is the capacitance of energy storage capacitor, R is the parallel resistor, L_K is core leakage inductance, L_P is primary core inductance, and L_1 and C_1 are the distributed inductance and capacitance of stalk per stack section length.
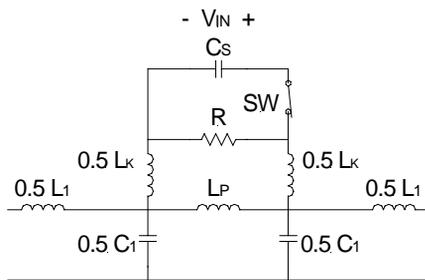

Figure 1: A symmetrical style single stack model.

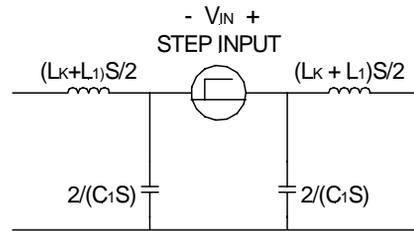Its corresponding simplified model derived in [2] is given in Figure 2.

Figure 2: A symmetrical style simplified single stack model of inductive voltage adder with step input.

NETWORK ANALYSIS AND DESIGN FORMULAS

The multi-stack inductive voltage adder model derived from single cell model is a ladder network of multiple "step input" sources.
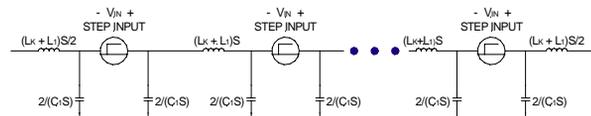

Figure 3: A symmetrical style simplified multi-stack model of inductive voltage adder with step input.

Since the ideal step voltage source shall have zero impedance, the network transmission impedance of inductive voltage adder is then given by

$$Z = \sqrt{\frac{L_K + L_1}{C_1}} \qquad (1)$$

This result shows that the circuit output impedance is larger than the stalk impedance due to the contribution of the leakage inductance. In order to minimize pulse reflections, the output cable and load shall match to the circuit output impedance Z rather then the stalk impedance.

The transmission delay time per stack cell is simply the propagation time of each transmission line section. It is given by

$$T_C = \sqrt{(L_1 + L_K)C_1} \qquad (2)$$

Each stack cell has a natural resonant frequency of

$$\omega_O = \frac{1}{\sqrt{(L_1 + L_K)C_1}} \qquad (3)$$

Commonly used configuration of inductive voltage adder is shown in Figure 4

Figure 4: Common configuration of multi-stack inductive voltage adder.

It is called a single-ended IVA, if one of the load, ZL or ZR, is a short and the other one is matched to IVA transmission impedance Z. It is called a double-ended IVA, if both loads are identical and equal and matched to IVA transmission impedance Z.

Assuming all step input here has a voltage V_{IN} as in previous section, and ZL is a short and ZR equals to Z. The load voltage of single-ended matched IVA can be expressed as

$$V_{load} = NV_{IN} \qquad (4)$$

Where V_{load} denotes output voltage across load ZR and N is number of stacks. Its response voltage or current rise time, T_R, of single-ended matched IVA can be expressed as

$$T_R = 2N\sqrt{(L_K + L_1)C_1} \qquad (5)$$

Similarly, the load voltage of either end, V_{Dload}, of double-ended matched IVA can be expressed as

$$V_{Dload} = \pm \frac{NV_{IN}}{2} \qquad (6)$$

Where, V_{Dload} is positive for ZR and negative for ZL. The load voltage or current rise time, T_{DR}, of a double-ended matched IVA can be expressed as

$$T_{RD} = N\sqrt{(L_K + L_1)C_1} \qquad (7)$$

Here C_1 and L_1 are stalk capacitance and inductance, and L_K is leakage inductance. They serve as transmission line elements during pulse propagation.

It is interesting to note distinctive differences of inductive-voltage-adder (IVA) and pulse-forming-network (PFN).

- The output voltage of IVA is linearly dependent of number of stack cells, but output voltage of PFN is independent of number of cells.
- The pulse rise time of IVA is linearly dependent of number of stack cells, but pulse rise time of PFN is independent of number of cells.
- The pulse length of IVA is independent of number of stack cells, but PFN pulse length is dependent of number of cells.

APPLICATION EXAMPLES

To demonstrate design application, we show a few simulation examples. Simulation parameters are from an actual circuit given in [3]. All switches are assumed to be ideal and identical.

TABLE 1: SIMULATION PARAMETERS

Symbol	Parameter	Quantity
C_S	storage capacitance	24×10^{-6} F
L_P	primary inductance	20.9×10^{-6} H
L_K	leakage inductance	6.5×10^{-9} H
L_1	stalk inductance per stake	20×10^{-9} H
C_1	stalk capacitance	2.6×10^{-12} F
N	number of stakes	30, 20, 10
V_0	initial voltage of C_S	1000 V
R	parallel resistance	50
Z_{STALK}	stalk impedance	50

From the above parameters, we can calculate the load impedance as

$$Z = \sqrt{\frac{L_K + L_1}{C_1}} = \sqrt{\frac{(6.5 + 20) \times 10^{-9}}{2.6 \times 10^{-12}}} = 100.96\,\Omega \quad (8)$$

Here, the calculated load impedance is about twice of the stalk impedance.

Assuming a single-ended 30 stack IVA where ZL is a short, the voltage pulse rise time across ZR can be estimated by using equation (5).

$$T_R = 2 \times 30\sqrt{(20 + 6.5) \times 2.6 \times 10^{-21}} = 15.75\,ns \quad (9)$$

Using equation (6), we have the estimated output load voltage of the single-ended IVA

$$V_{load} = 30 \times 1000\,V = 30\,kV \qquad (10)$$

The simulation result is in Figure 5. A comparison of matched and mismatched impedance cases are shown in Figure 6, which illustrate effects on pulse waveforms.
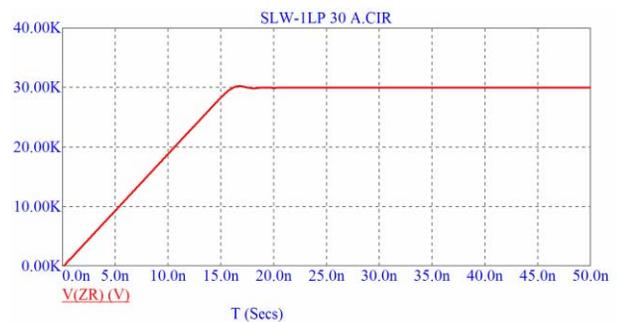

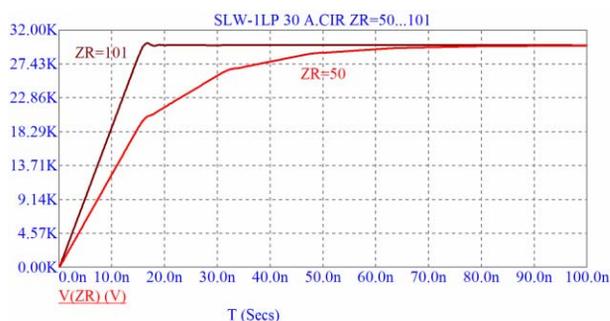Figure 5: The output pulse waveform of a 30-stack single-ended IVA.

Figure 6: Output pulse waveforms of a 30-stack single-ended IVA with matched or mismatched impedance.

Here we shown a set of simulation examples of double-ended IVA of 10, 20, or 30 stacks with switch on at 0.1 ns and off at 40 ns. The estimated parameters shown in Table 2 are calculated using equations given in the previous section. Simulation results and estimated parameters are well agreed.

TABLE 2: ESTIMATED DESIGN PARAMETERS

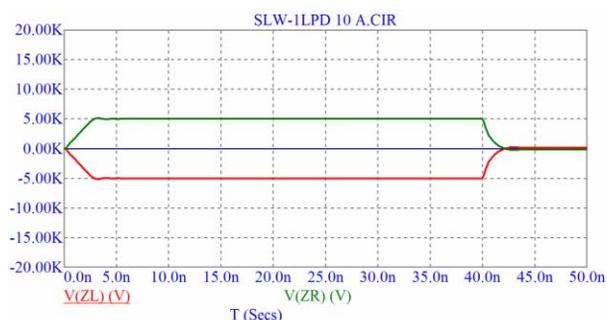| Symbol	Parameter	Quantity			
N	Number of stacks	10	20	30	
T_{RD}	Pulse rise time				ns
V_{Dload}	Pulse voltage				kV

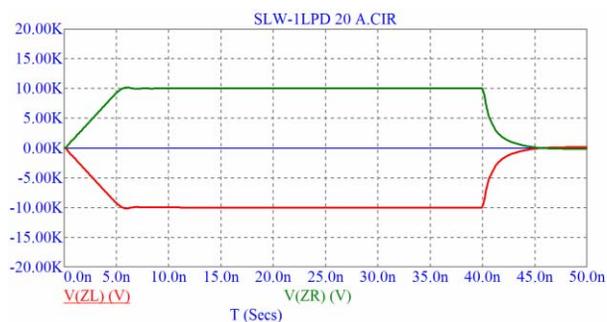Figure 7: Output pulse waveforms of a 10-stack double-ended IVA.

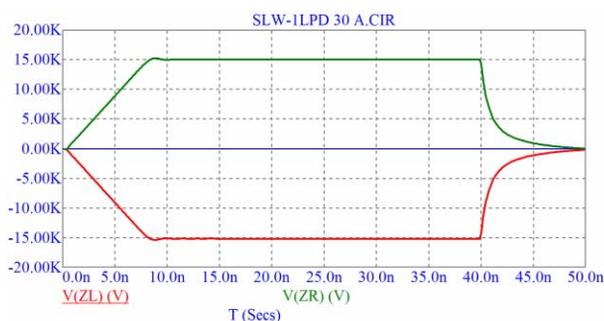Figure 8: Output pulse waveforms of a 20-stack double-ended IVA.

Figure 9: Output pulse waveforms of a 30-stack double-ended IVA.

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