PHASE SYNCHRONIZATION OF MULTI-NETWORK SYSTEM FOR RESONANT EXCITATION OF THE JHF 3-GeV BOOSTER MAGNETS

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Abstract

In the Japan Hadron Facility (JHF), the 3-GeV booster is planned to be a 25 Hz rapid cycling separated-function synchrotron. To achieve a stable acceleration, the tune variation due to tracking errors is required to be less than 0.01. Since the White-circuit is adopted with a pulse power supply as its ac source, the relative phase difference of multi-network field becomes one of the main causes of the tune errors and should be minimized. The tolerable phase shift is estimated to be 0.8 mrad. This paper describes a scheme to synchronize the multi-network excitation. A circuit for phase feedback is implemented and experimental results are presented.

1 INTRODUCTION

Rapid cycling synchrotrons of separated function have come into use in several facilities such as ESRF 10 Hz booster [1] and BESSY II 10 Hz booster [2]. In the Japan Hadron Facility (JHF), the 3-GeV booster is designed to be a 25 Hz rapid cycling separated-function synchrotron [3], in which the tune variation due to tracking errors is required to be less than 0.01 to achieve a stable acceleration. Resonant magnet excitation using White circuit powered by biased ac power source is the traditional configuration for rapid cycling synchrotrons. In separated-function machines, tracking errors are caused by high harmonics in resonant magnet current and phase errors between multi-networks. We have built two model networks powered by traditional pulse ac sources to examine the phase synchronization [3]. We designed a phase feedback circuit to achieve the phase synchronization.

2 PHASE ADJUSTMENT SCHEME

A phase adjustment circuit is implemented to synchronize the resonant current in the slave circuit with the master one as shown in Fig.1.

2.1 System Configuration

Two model resonant networks (L_m, C_m) and their pulse ac sources are shown in Fig.1. The upper set is operated as master system while the lower one as slave one.

Half-sine-like current pulses (I_p) are generated by triggering the pulse thyristors (SCR) in the pulse ac sources.
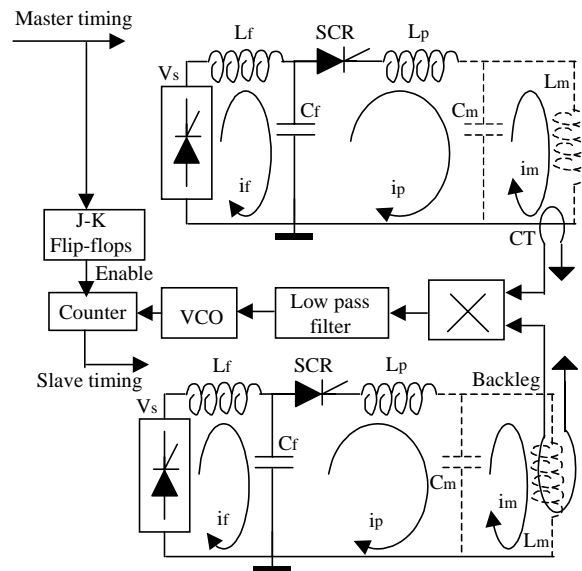

Figure 1: Configuration of multi-network system with a phase synchronizing system.

The phase synchronization of the resonant currents (I_m) is performed by adjusting the slave timing with respect to the master timing for the pulse SCR triggerings. As shown in Fig.1, a mutiplier and low-pass filter detect the phase difference between the master and slave resonant currents. The phase difference is converted to a dynamic dc voltage, and it is used to adjust the frequency of a voltage-controlled oscillator (VCO). Since the slave timing is obtained by counting the VCO pulses, it is regulated automatically by feedback to achieve a close tracking between the resonant currents (I_m) of the two resonant networks.

2.2 Phase Regulating Circuit

The simplified circuit for phase regulation is shown in Fig.2. The master timing is utilized as the synchronization clock for the system operation. The falling edge of the master timing pulse triggers the flip-flop to deliver the enable signal to start the counter. The VCO frequency varies with the changing phase difference around the

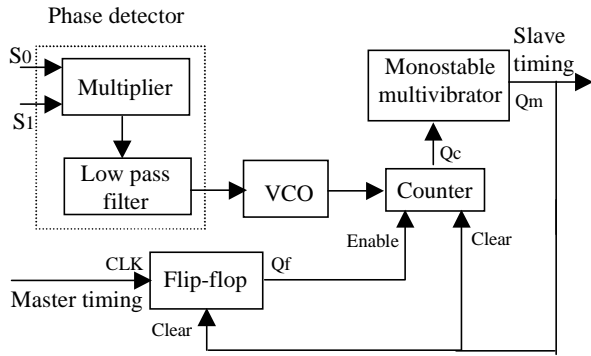centre-frequency set by a bias voltage. Counting the VCO pulses regulates the slave timing.

Figure 2: Simplified circuit for the phase regulation.

Since a high tracking accuracy between the master and the slave is required, the phase detector should be sensitive to a very small change of the phase difference ($\Delta\varphi$). The multiplier phase detector is adopted. Taking into account the phase of resonant current with respect to the gating signal of the pulse SCR, we choose S0 the master resonant current picked by a CT (current transformer) but S1 the backleg signal of the slave magnet load. Thus the output signal from the low-pass filter depends on $\sin(\Delta\varphi)$, which is approximated as $\Delta\varphi$.
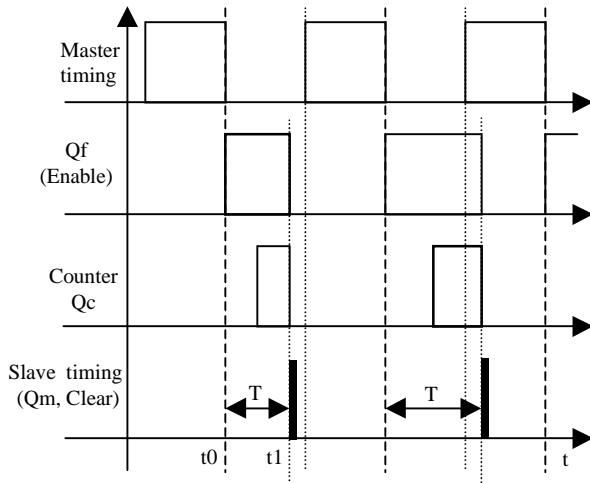

Figure 3: Time diagram of the phase regulation circuit.

As shown in Fig.3, the master timing, with a duty factor of 50%, triggers the negative-edge flip-flop to give the enable signal for the counter to start counting at t0. When the counting ends at t1, the falling edge of Qc produces a one-shot signal Qm that is used as the slave timing and the counting is disabled. As the result, the slave timing (rising edge) is produced either leading or lagging the master timing according to the counting duration T as illustrated in Fig.3.

2.3 Parameters and Functions

Basic parameters of the pulse sources and the resonant networks are given below.

Pulse or resonant frequency, f_p : 50 Hz

Energy-storage capacitor, C_f : 23 μF

Filter choke, L_f : 7 H

Pulse choke, L_p : 49 mH

Magnet inductance, L_m : 10 mH

Resonant capacitor, C_m : 1 mF

Quality value of resonant network, Q: 75.

The block diagram shown in Fig. 4 describes the system implementation of the phase adjustment.
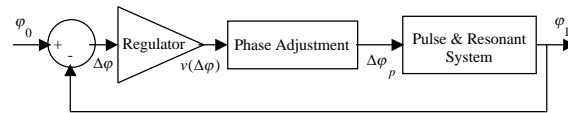

Figure 4: Diagram of the phase adjustment system.

As shown in the figure, $\Delta\varphi$ is the phase difference of the resonant currents (I_m) between the slave and master networks. The phase of the pulse current (I_p) in the slave system is adjusted dynamically according to the variation of $\Delta\varphi$. Since the phase of the resonant current is dependent on triggering timing of the pulse SCR around the resonant frequency, the phase of the resonant current (φ_1) in the slave system is regulated accordingly to be synchronized with the master phase (φ_0).

The phase adjustment is realised by counting the VCO pulses as described above. The VCO centre frequency is given by:

$$f_0 = 2f_p N \ ,$$

where f_p is the pulse frequency given by the master timing, $N = 2^{16}$ is the counter length of a 16-bit counter. Both the phase adjustment and the pulse & resonant system can be approximated by simple proportional elements. A PI (Proportional, Integral) regulator can be used to achieve dc stability in φ_1. A simple proportional element is used as the regulator in the experiment.

3 EXPERIMENTAL RESULTS

The system can be operated in free or feedback mode. In free mode, the phase of the slave resonant current can be adjusted freely by changing the VCO bias-voltage. In

feedback mode, phase regulation and synchronization is carried out automatically by the phase feedback. In both modes, reliable operations have been done. With phase feedback, the phase synchronization is performed with a satisfied accuracy in long-term.
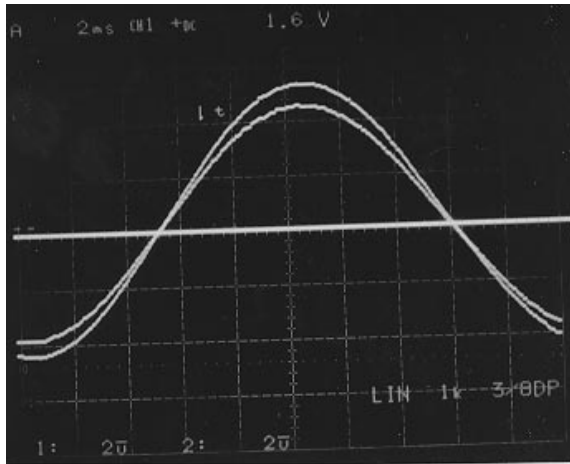

Figure 5(a): Synchronized resonant currents, 2 ms/div.

Figure 5(a) is a photo showing the synchronized resonant currents of the master and slave networks. The phase difference is obtained by comparing their zero-cross signals with a phase-comparator. Figure 5(b) gives the phase-comparator pulse. In Fig. 5(b), we recorded numerous shots, which show that the phases are synchronized within 1 us momentarily.
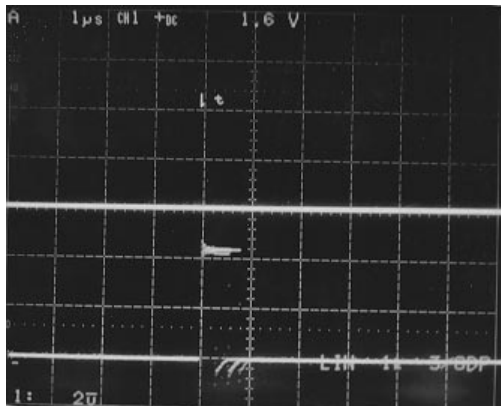

Figure 5(b): Phase difference pulse, 1 us/div.

To measure the long term precision of the phase synchronization, the pulse-width of the phase-comparator output is converted to a voltage level by an integrator - holder circuit, which has a conversion ratio of 1us/10mV. This voltage is measured with a multimeter (Hp3458) and recorded with Hp-VEE via Hp-IB bus. Figure 6 gives the result measured during 8-hours (1measurement /4second, 7200 measurements in total). In the measurement, the

slave timing is shifted about 2 us intentionally so that the full variation of the phase difference can be viewed.
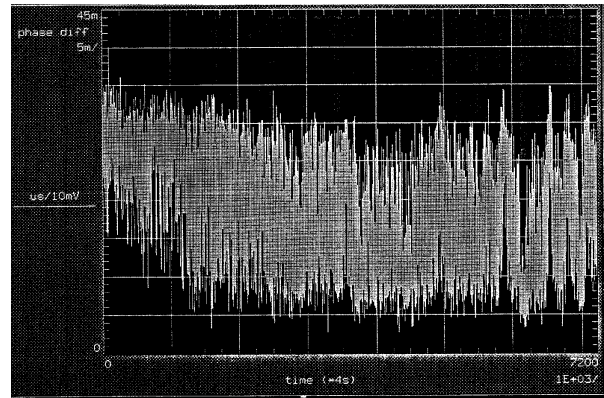

Figure 6: Result of the long-term precision of the phase synchronization, phase difference: 0.5 us/div.

The experiment has shown that a high precision of the phase synchronization is achieved and the variation of phase difference is kept within about 3 us in the 50 Hz resonant system. If applied to 25 Hz system, a precision less than 6 us, which is equivalent to 0.94 mrad, can be expected.

4 CONCLUSIONS

This experimental study shows that using a pulse power supply is still feasible to achieve a high tracking accuracy in rapid-cycling synchrotrons with separated-function. In the experiment, the phase synchronization almost reached the accuracy required by the JHF booster design. In the same time, new concept of ac power sources, e.g. BESSY-II type [2], is also expected to apply in the JHF booster synchrotron to avoid the intrinsic disadvantages of pulse ac sources. An IGBT inverter of the BESSY-II type to power the White circuit is under development.

5 ACKNOWLEDGMENTS

6 REFERENCES

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