# V123 BEAM SYNCHRONOUS ENCODER MODULE*

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*Abstract*

The V123 Synchronous Encoder Module transmits events to distributed trigger modules and embedded decoders around the RHIC rings where they are used to provide beam instrumentation triggers [1,2,3]. The RHIC beam synchronous event link hardware is mainly comprised of three VMEbus board designs, the central input modules (V201), and encoder modules (V123), and the distributed trigger modules (V124). Two beam synchronous links, one for each ring, are distributed via fiberoptics and fanned out via twisted wire pair cables. The V123 synchronizes with the RF system clock derived from the beam bucket frequency and a revolution fiducial pulse. The RF system clock is used to create the beam synchronous event link carrier and events are synchronized with the rotation fiducial. A low jitter RF clock is later recovered from this carrier by phase lock loops in the trigger modules. Prioritized hardware and software triggers fill up to 15 beam event code transmission slots per revolution while tracking the ramping RF acceleration frequency and storage frequency. The revolution fiducial event is always the first event transmitted which is used to synchronize the firing of the abort kicker and to locate the first bucket for decoders distributed about the ring.

## 1 BEAM SYNCHRONOUS EVENT LINK SYSTEM ARCHITECTURE

The RHIC collider is composed of counter-rotating particle beams in two 3.8 km super-conducting rings which will be collided in four of the six interaction regions. There are two RHIC beam synchronous event encoding systems; one for each ring. Each beam synchronous event system is the same; therefore only one system will be described. Both RHIC beam synchronous event encoding systems are located in the 4 o'clock equipment house 1004A in a single VME chassis. Each beam synchronous event encoder system requires five VME chassis slots, one for the V123 master module, and four for the V201 input modules. The beam synchronous event link carrier tracks a varying 14.07 MHz RF clock, derived from half the RHIC injection and acceleration RF frequencies. A synchro-synthesizer board in an RF system chassis is the source of this RF clock. The beam synchronous event link is initiated as differential transformer coupled PECL, and connects to a 1 x 8 ECL fan out module then to 6 fiber optic transmitters. The transmitters drive single mode 9/125 μm fiber optic lines to 6 service buildings in a star configuration where they are passively split out to the 18 ring alcoves and 4 experimental halls. Each alcove has 2 beam synchronous fiber spools, one for each ring. Alcoves, and equipment houses have spools of fiber optic cable located at receiving locations to equalize the transmission delays. At an alcove, the fiber optic transmission is converted to differential ECL and fanned out by 1 x 8 ECL fan-outs to the V124 modules and embedded decoders in the beam position monitors. The output of the V124 modules may be used directly or fanned out by 1 x 8 fan out units with LEMO KLOC connectors where these signals are finally used by instrumentation triggers and experiments.

## 2 PURPOSE

The low jitter PLL [4] recovered clocks are intended to provide precise timing and synchronization information to instrumentation triggers and data acquisition systems used in experiments and for general beam bucket phasing purposes. Prioritized hardware and software triggered inputs can be output to any of 256 event codes after translation in a SRAM look-up table. There are a total of 15 event slots per revolution. The revolution event will have the highest priority and will always be output at the beginning of the revolution cycle. The event codes are decoded and used by devices such as extraction kickers, and as a reference for timing triggers and delayed timing triggers. Other beam synchronous events will be sent on an input prioritized basis, but can be delayed by the revolution event. Since the link is fanned out in a star configuration with equalized delays, an event will arrive simultaneously at all locations around the ring with nanosecond precision, and sub-nanosecond jitter. Programmable delays are provided by the V124 distributed trigger modules using the beam sync link recovered clock. Counters running on this clock will synchronize to the revolution event. The recovered low jitter distributed clock is the basis for the timing precision of the beam synchronous system. The passage of any and all bunches around the ring can be signaled precisely to sub-nanosecond resolution.

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## 3 SYSTEM OPERATIONAL REQUIREMENTS

The beam revolution time is approximately 12.78 μs, or 78.196 k revolutions/second. The number of RF buckets per revolution is 360. From these data, a 28.15 MHz RF bucket frequency is derived. The beam synchronous event encoder requires a 2X clock to produce the bi-phase mark data stream. The beam synchronous encoder receives the RF 28.15 MHz clock and derives the 14.07 MHz beam synchronous event link. The RF system generates the 2X clock and revolution tick during RHIC operation. The revolution tick performs two functions: first it sets the phase of the beam synchronous event link bi-phase clock, and second it synchronizes the revolution tick event code. A 28.15 MHz crystal backup clock oscillator can provide an event link output when the RF clock and tick isn't available. A control register bit can control cancellation of automatic switching.

### *3.1 Revolution Fiducial*

The most important event transmitted by the V123 beam synchronous event encoder is the revolution fiducial. This fiducial is sent synchronously with the revolution tick provided by the RF system synchro synthesizer module. The revolution tick is derived from the first bucket passing the 4 o'clock RF wall current monitor. The revolution event always occupies the first event slot which is synchronized by the revolution tick. If the tick synchronization is removed or lost, the V123 counters will continue to send the revolution event every 360 cycles of the RF clock. Should the revolution tick not occur after 360 clock cycles or occur before or after this count an interrupt is generated and the synchronization loss error is flagged. A crystal backup clock oscillator may be used to provide a beam sync link carrier and revolution event code for testing purposes when no rf input signals are present.

### *3.2 Beam Dump - Abort Kicker Timing*

Prior to the revolution tick there are approximately 18 empty RF buckets. These empty buckets accommodate the abort kicker rise time, which is about 700 ns [5]. The abort kicker logic monitors the Beam Sync link for the rotation fiducial. All requests to abort the beam are synchronized to the rotation fiducial followed by an appropriate delay to properly time the kicker firing trigger with the abort gap.

### *3.3 Encoding*

The beam synchronous event codes are transmitted using a serial modified Manchester code (bi-phase-mark). This modulation technique guarantees a signal level transition at each cell edge, rather than the cell center as is done in the true Manchester code (also bi-phase-mark). A "one" is defined as a level transition in the cell center, while no center transition is a "zero". There are 180 bi-phase cells per revolution, and 12 bi-phase cells per event transmission. This allows 15 event slots per revolution, of which 1 to all may be filled.

During idle periods, the beam synchronous event line contains continuous bi-phase-mark "ones" (14 MHz square wave) transmission, with a single revolution tick event once a revolution. Even parity is selected so that idle "ones" bi-phase cells always start with a positive, rising edge, transition at the V123 module output. A single beam synchronous event code transmission, which requires approximately 0.853 ms, is shown in figure 1.

## 4 V123 MODULE FEATURES

- FLEX® 10K [6] FPGA based design
- SRAM translation table
- Input error interrupts
- Change of status interrupts
- Re-synch error detection
- VME Interface
- VMEbus cycle stealing
- VMEID
- FIFO

### *4.1 FLEX®10K FPGA based design*

An Altera EPF10K10QC208-3 is used in this design because it has 3 EAB blocks that are used for SRAM, ROM, and FIFO without the need for external devices.

### *4.2 SRAM translation table*

The 256 x 8 SRAM table in the Altera FLEX10K EAB block acts as a trigger to event translation table. Any trigger can be mapped to any event code.

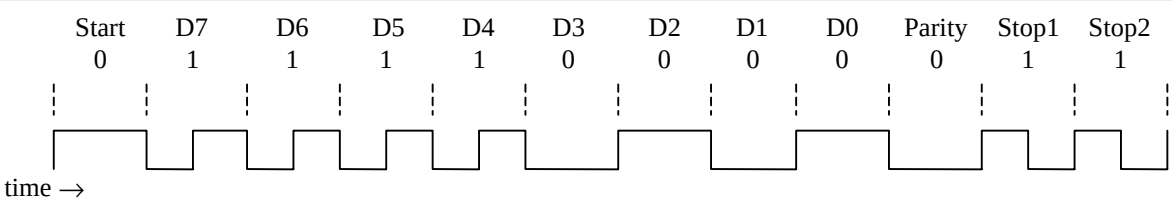


Figure 1: Modified Manchester event frame

### *4.3 Input error interrupts*

If an event trigger code is received from the V201 input modules which is not one of the 63 allowed on this input, an out of range error interrupt is flagged.

### *4.4 Change of status interrupts*

Two interrupts monitor the RF and beam tick inputs. If a signal is removed or reconnected an interrupt will be generated. The RF input is monitored for carrier. The beam tick input is monitored for phase relationship. Addition or deletion of this input will cause an interrupt.

### *4.5 Re-synch error detection*

Any time a beam tick is received out of sequence, an error is flagged. This bit will not be set unless an error or discontinuity in the input signals is received.

### *4.6 VME Interface*

The VME interface is A24, D08(OE). Interrupts are supported with a programmable interrupt vector and IRQ level. The SRAM lookup table, and all control and status registers are accessible through this interface. Each board occupies a 4K address block in the A24 space. The four V201 input modules occupy 64 addresses in sequential order from this base address, by having the V123 address decoder signal accessible on the dedicated P2 backplane.

### *4.7 VMEbus cycle stealing*

The V123 shares access to its SRAM lookup table between the translation requirement of the output encoder and the VMEbus. If all transmission slots were filled, the translator would operate 100% of the time eventually causing a VME bus error to occur after a timeout. To ensure that the VMEbus is serviced with a full complement of trigger events from either the input triggers or batched through the FIFO, cycle stealing is employed. A portion of the encoder time which processes the framing start and stop bits need not access the SRAM, VMEbus read and write cycles are completed during this time.

### *4.8 VMEID*

A 64-bit VMEID ASCII string is saved in the ROM implemented in one of the 3 EAB blocks in the Altera chip. This string is used by the front-end computer to identify the board in the VME chassis, and its revision. This information is checked at initialization.

### *4.9 FIFO*

Software events are the lowest priority triggers. These events are processed last after other input triggers. A FIFO is necessary to preserve these events for the first available opening when no other triggers are active. The highest priority is the revolution event, followed by the 64 prioritized hardware triggers from the V201 followed by the events stored in FIFO. The FIFO may be used to batch events. An input filter prevents trigger values less than 64 from being written to the FIFO. This prevents the use of higher priority input trigger codes from being translated to lower priority FIFO events unless they are multiply mapped.

## 5 ACKNOWLEDGMENTS

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[6]FLEX is a registered trademark of Altera Corporation.