INTEGRATED SOFTWARE ENVIRONMENT OF LONGITUDINAL FEEDBACK SYSTEM FOR TLS

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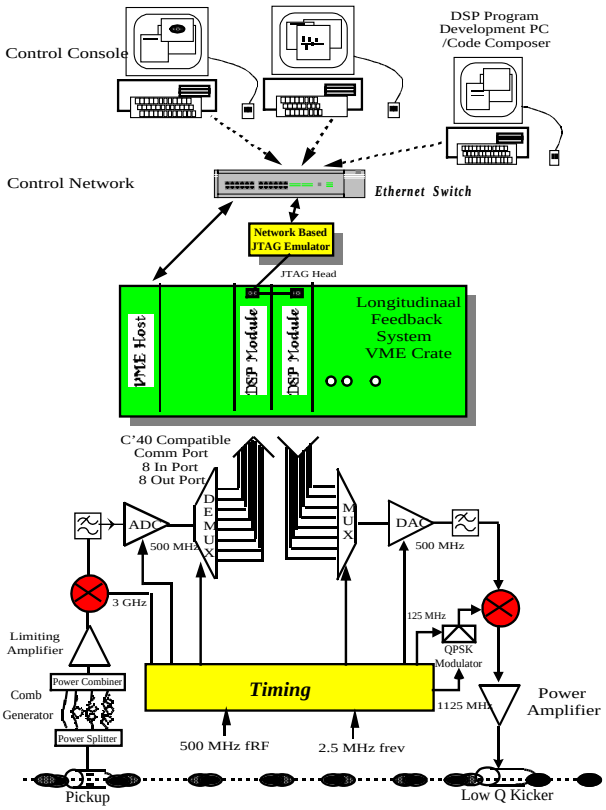
Abstract

A DSP based longitudinal multi-bunch feedback system is being developed in SRRC, The software structure of feedback consist of a digital signal processors array to execute feedback algorithm and to provide raw data for beam diagnostic purposes. In order to develop, commission and operate this system efficiently, an integrated software environment has been developed. In such environment, we have major software components including, (1) feedback control algorithm on DSP, (2) DSP developing environment is on PC, (3) diagnostics toolkits is on PC and embedded computer, (4) operator interface on PC and workstation. The feedback control loop is a combined with digital filter and controller. DSP developing environment includes a code composer running on PC as well as a remote Ethernet based JTAG emulator to debug program. The system will equip diagnostic toolkits to acquire and analyse data. The associated hardware and software are commercial products that may help to reduce the system development time. The design features and performance of such will be reported

1 INTRODUCTION

A digital longitudinal damper is being developed in SRRC to stabilise the longitudinal coupled-bunch instabilities observed in the TLS storage ring [1]. It is a bunch by bunch feedback system designed for 200 bunches at 2 ns bunch interval. The longitudinal feedback (LFB) system in SRRC consists of five parts. The front-end RF electronic system, data input and output system, data processing and low-Q kicker. The Commercial Off-the-Shelf (COTS) extensive product solutions are used in DSP to reduce development times. Designs of the bunch phase detection circuit, the digital electronics and the 1125 MHz wide-band RF system for correction of phase errors have been tested with the beam. The core of the digital electronics is a DSP array that utility DSP modules performing parallel processing at a data throughput of 500 Mbytes/sec. This COTS products take off the expense and risk of in-house development, A prototype operating at one eighth of the data rate of the final system is under construct to evaluate the system design.

Figure 1: System diagram



2 LFB SYSTEM ARCHITECTURE

The data processing is divided to two major parts. One is data communication, other is digital signal processing and development system. The data transportation is by the C'40 compatible communication ports of digital processing unit. There are eight input ports and eight output ports in this system. The digital processing unit is consists of VME hosts, DSP modules and JTAG emulator.

2.1 LFB electronics

The longitudinal feedback (LFB) system in SRRC is separated to five parts. The ADC/DEMUX and DAC/MUX circuits with peak data transfer rate of 500 Mbytes/s. The ADC/DEMUX board digitises the discrete phase error signal for search bunches at 500 MHz and

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distributes to the processors that have slower clock rate for signal filtering. By using the DAC/MUX board, the filtered signals from the processors are then combined in correct sequence and converted into a single analog signal (the correction signal). The signal is amplified up to 200 Watts, and the RF power amplifier is used to drive the longitudinal kicker that in turn kicks individual bunches every 2 nanoseconds. The RF system consists of the 3 GHz prompt bunch phase detection unit, and the 1.0-1.25GHz broad band drive chain is used to drive kicker [2,3].

2.2 Data throughput considerations

The front-end electronics sample the data in 500 Mbytes/sec. Decimate factor is 18 in present system configuration. Another decimation factor is possible. Bunch oscillation is sampled at one turn, the following consecution 17 turns data is omitted. The communication ports, use in the LFB system as a unidirection communication interface to bunch oscillation detector and kicker system. A communication port sends or reads each of the stored words in its FIFO on a byte-to-byte basis. The separated input and output COMM port support 20 Mbytes per second. The transfer time is 1.4 us in each twenty-five bunch. Performance of communication port is satisfied with the requirement of LFB system.

2.2 DSP modules

There are two kinds of DSP modules. One is TMS320C4x, another is TMS320C6x. In prototype test, TMS320C4x are used. The TMS320C4x can deliver up to 30 MIPS/60 MFLOPS performance with a maximum I/O bandwidth of 384M bytes/s. However, data type in LFB system is byte oriented, floating point features in ‘C40 is useless. High MIPS integer DSP is preferred for LFB application. The TMS320C6x is upgraded processor in LFB system. There is 1600 MIPS and 200 MHz (5 ns instruction cycle time) in C6x. Advanced VelociTI VLIW architecture that enables sustained throughput of up to eight instructions in parallel. New development paradigm is based on software, not hardware. C6x DSPs use RISC-like instructions, which facilitate mapping to multiple functional units for additional scheduling flexibility. It is very efficient for LFB system on filtering operation, especially.

3 SOFTWARE ENVIRONMENT

3.1 DSP software development environment

This development system is an Ethernet based JTAG emulator. It is able to remote control by local computer with window user interface in windows95/NT operation system. It supports to multi-processor download and develops DSP program in the same time. The code composer is a system development tool that supports an integrated development environment (IDE) for C4x and C6x. This environment allows DSP code designer to edit, build, manage products, debug and profile from a single application. In addition, the IDE lets user compile in the background as well as analyze signals graphically (including Eye Diagnostic. Constellation Diagnostic. FFT Waterfall, Image display etc.), perform file I/O, debug multiprocessors, and customise a C-interpretative scripting language in the IDE.

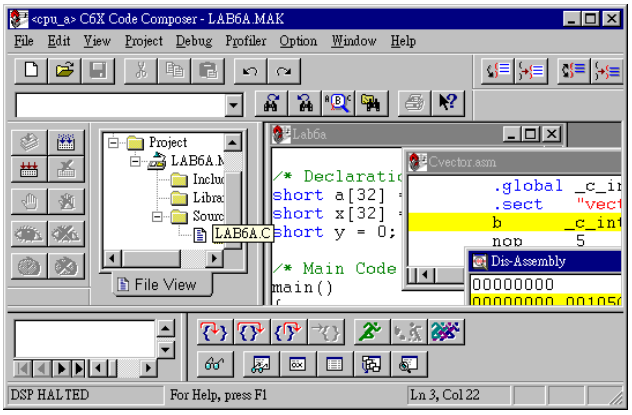

Figure 2: Development tool.

3.2 Feedback software

All tasks of feedback software are optimal for communication and filtering. This task can’t be swapped when processor is accessing from COMM port memory. The phase shift, and band-pass filter tasks are embedded in DSP module. In the meantime, it receive filter control and feedback status control from host. The DSP modules include of multiprocessors to process input data, to kick system.

3.3 Host

The tasks of host are embedded in VME controller, are connected with console computer to support to feedback remote control, filter coefficient update, status reports and data analysis. The relationship tasks are shown in figure 3. The setting service handles filter and status control. General reading handles raw data store.

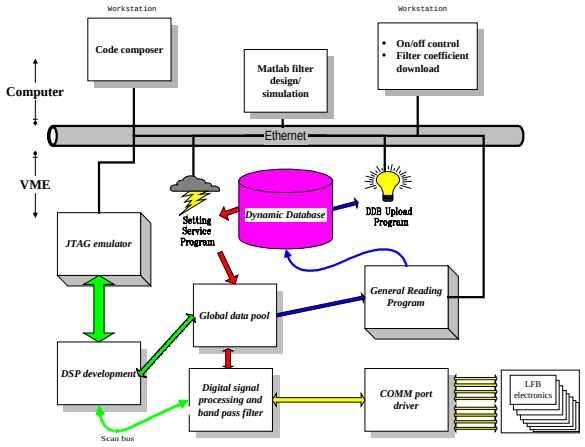

Figure 3: Relationship between software components

3.4 System management

There are many tasks in host that is necessary to be managed, for diagnostic request. These tasks include of download filter coefficient, on/off control, and save raw data. For example, feedback is necessary to be stopped when host is updating filter coefficient. and then re-turn on feedback. Status control task has lower priority than filter control.

3.5 Console software

There are several tools in console except for development tool, such as, filter simulation and raw data on line display. An integrated MATLAB simulation tool is applied in console. To support to various conditions in commission, adjust phase and centre frequency of band-pass filter on online that is efficient. The 200 samples will equally distribute via eight C'40 COMM ports to DSP modules. Every COMM port handles twenty-five bunches data. Current design use synchronous data transfer scheme, i. e. All data is collected, and then is blocked filtering [3]. The cycle time of output via out component is 7.2 us, 25 bunches data is parted to 28 bytes, and transfer to DSP module via COMM port. The data transfer time is about 2 us. Peak data throughput is about 10 Mbytes/sec per COMM port.

5 CURRENT STATUS AND FUTURE WORKS

The preliminary test has suppressed longitudinal oscillation successfully. The analog input of LFB electronics has been connected with COMM port of processors. This testing is a single bunch longitudinal oscillation that is suppressed by the feedback loop and RF cavity [5]. The oscillation frequency is destroyed when feedback is turned on. The band-pass filter will be improved to infinite impulse response filter. There is narrower bandwidth than FIR filter in the same tap. The parts of LFB electronics are still in implementation stage. The analog input electronics have been finished testing. The processors are successfully connected with this board. The analog output electronics is designing now. The data transformation is by JTAG port now. The process will be paused when data is sending with JTAG port. The software for the control in the longitudinal feedback system has been developed with COTS product.

In the future, Feedback software will be developed continuously software and to aid commission of the system.

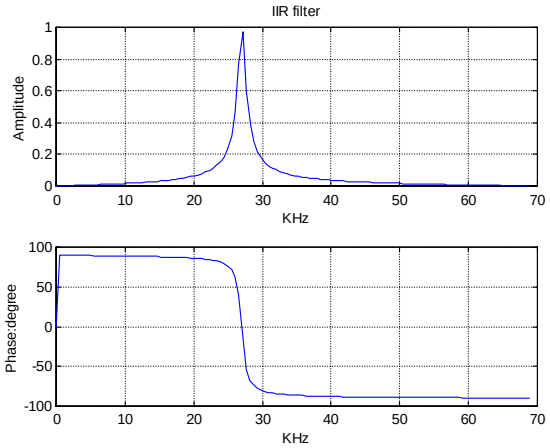

Figure 4: IIR filter simulation.

6 REFERENCE

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