

# Enhanced functionality and Performance of the Longitudinal Damping System at the ALS\* using a New VXI Based Processing System\*

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## Abstract

The ALS longitudinal feedback electronics, designed and developed at the Stanford Linear Accelerator center (SLAC), has been operating very reliably at the ALS for over four years [1]. Recently a new VXI based implementation of the entire RF and timing electronics has been built, tested, and will soon replace an earlier prototype installation. The components designed are contained in three VXI packages along with a VXI controlled system oscillator chassis. The new system contains a number of functional enhancements that most notably include: enhanced timing control, internal temperature monitoring of all VXI modules, simulated beam signal generation, automatic locking of the phase detector servo loop, and the monitoring and alarm of critical RF signal levels. The details of the design and implementation of the VXI modules along with performance characteristics are presented below.

## 1 INTRODUCTION

The longitudinal multi-bunch feedback (LFB) system currently in operation at the Advanced Light Source (ALS) was a “first version” demonstration unit designed as part of a multi-lab collaboration for use at the ALS, PEP-II, and DAΦNE machines. Since the commissioning of the ALS damping system a number of VXI based modules especially for the RF and timing sections have been designed and constructed for the PEP-II [2] machine to enhance operational reliability and equipment problem analysis. Early versions of these modules have been constructed and debugged for the ALS system and are now ready for installation.

## 2 OVERVIEW OF LFB SYSTEM

The LFB system was designed to suppress longitudinal coupled bunch instabilities in the PEP-II and ALS electron storage rings. The basic scheme is a bunch-by-bunch feedback system that measures the instantaneous phase error of each bunch with respect to the average bunch synchronous phase. The system then applies a delayed longitudinal correction voltage to each

identical bunch through a low Q multiple gap drift tube kicker structure [3].

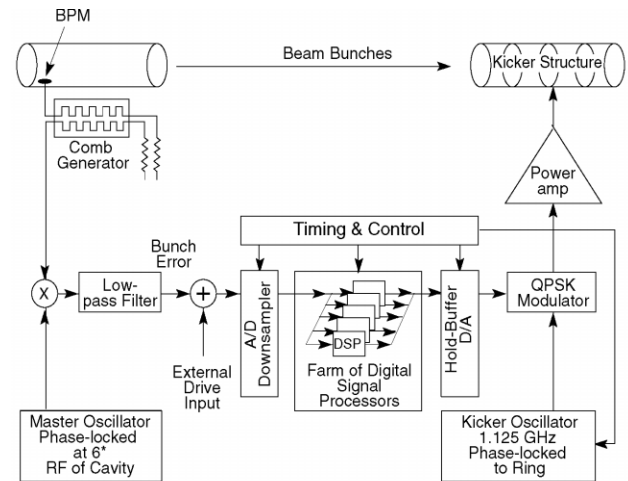


Figure 1 Block Diagram of the Longitudinal Feedback System

As shown in fig 1 the longitudinal beam bunch phase motion (error signal) is initially detected through a precisely balanced four button beam position monitor (BPM) at the 6th harmonic (3.0 GHz) of the ALS cavity RF. A passive “comb type” band pass filter with a 4 cycle ‘tone burst’ response creates a precisely defined bunch phase error signal and reduces the inter-bunch phase motion crosstalk. The  $6 \times \text{RF}$  (3.0 GHz) ‘front-end’ phase detector down-converts the beam signal to a base band (DC to 500 MHz) which contains all the coupled-bunch modes of beam motion. The resultant signal is digitised at 500 MHz, downsampled (by a factor of 24 for the ALS), tagged, and packed for serial transmission to the digital signal processor (DSP) array in the ‘down sampler’ module [4][5]. The low frequency of the coupled bunch instabilities ( $< 20$  kHz) allows for a distributed array of 40 DSP’s (4 per DSP module) to apply a tailored 6 tap FIR algorithm to each and every bunch. The resultant digital correction words are repacked and serially transmitted to a high speed (500 MHz) circular memory in the ‘hold buffer’ module. The converted analog output signal amplitude modulates (AM) a quadrature phase shift keyed (QPSK) carrier generated by the ‘back-end’ module. The QPSK carrier signal centred at 1.125 GHz ( $9/4^{\text{th}}$  of ALS RF) was chosen to accommodate the electrodynamic dimensions of the kicker structure and commercially available power amplifiers. Reference signals for the front and back end modules are generated

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in the System Oscillator chassis. Timing signals for the digital cards are generated in the timing module [6].

The RF, timing, and high speed digital modules have been packaged in RF tight VXI modules and adhere to the VXI standard interface. The DSP modules are packaged in a VME format. All electronic systems are directly controlled through a VXWorks real time operating system that is linked to an extensive EPICS graphical interface [7].

### 3 RF AND TIMING SYSTEM

#### 3.1 Front End Module:

The front-end VXI module as shown in fig. 2 contains a phase detector, low frequency DC phase servo loop, an RMS beam motion detector and appropriate signal monitor points. The phase detector baseband output is bandpass limited (< 500 MHz) to further reduce inter-bunch phase motion crosstalk. A signal splitter provides a feedback signal to a series pair of SLAC designed phase shifters that are connected to form a phase servo loop. The loop corrects for slow DC drifts in the average synchronous bunch phase and compensates for any thermal drifts in the front-end electronics. The beam motion detector provides a signal to the EPICS panel display that mimics the synchronous phase motion of the beam. Additionally an amplitude level can also be chosen to trigger a visual alarm. These two features provide a machine operator with a clear 'loss of lock' indication without the need to tie up an expensive monitoring oscilloscope. A useful software enhancement that is made possible through the new 'front end' hardware is the inclusion of an auto zeroing routine for the phase servo loop.

For normal machine set-up or occasionally after an RF cavity trip the 'front end' phase servo loop will have to be opened and re-locked. The process is simple and can be accomplished automatically (auto zero and lock) from the EPICS panel, or manually from the front panel of the VXI module in the equipment rack.

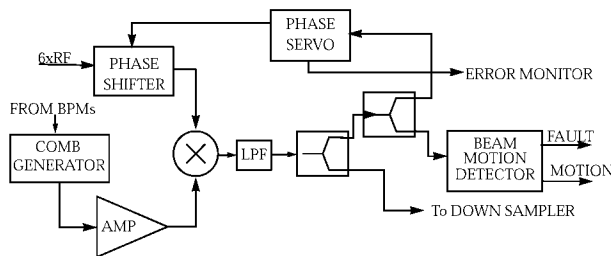


Figure 2. Block Diagram of Front-end module.

#### 3.2 Back End Module:

The back-end VXI module as shown in fig. 3 contains a QPSK modulator, amplitude modulator, RMS kick

output detector, QPSK test mode circuits, and appropriate signal monitor points.

The QPSK modulator impresses a 90 deg. phase shift every 2 NS on the 1.125 GHz ( $9/4^{th} * RF$ ) carrier signal for the kicker electrode. The phase of the carrier is synchronised to provide the proper accelerating/decelerating voltage to the specific bunch within the kicker electrode gap.

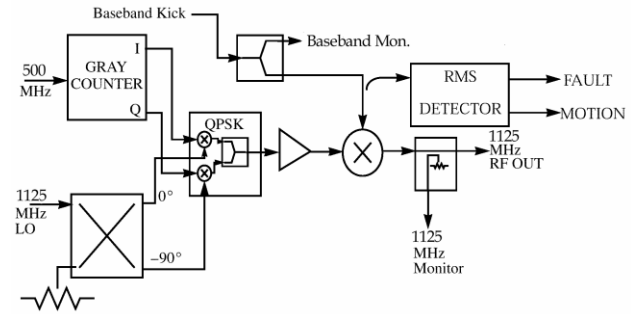


Figure 3 Block diagram of Back-end module

The in-line AM modulator, driven by the DSP generated baseband kick signal for each bunch, determines the amplitude and polarity of the correction voltage to be applied to the bunch within the electrode gaps.

The RMS kick output detector provides a signal to an EPICS panel display that is proportional to the kick amplitude required to damp the bunch train. This signal is a key system indicator that can confirm the loss of feedback lock, mode zero instabilities in the cavity, or back-end timing misalignment and again obviates the need of an external monitoring oscilloscope.

The QPSK test mode circuit can force the modulator to halt at one of four (0,90,180,270 deg.) selected phases. This feature provides a direct test of the QPSK modulator and provides a single tone test of AM modulator and the following amplifier chain.

#### 3.3 System Oscillator chassis and Breakout panel:

The System oscillator (SO) chassis generates the 3.0 GHz ( $6 * RF$ ) mixing and 1.125 GHz ( $9/4 * RF$ ) carrier signals for the Front and Back-end modules, houses the front-end comb filter, generates a simulated beam signal, provides real time monitoring and alarm functions of critical signals, and contains all the appropriate monitor points for expeditious hardware checkouts. The S.O. electronics is contained in a 19"x83/4"x24" rack mounted chassis that is connected to the EPICS/VXWorks software through a VXI interface card located in the chassis.

All the S.O. signals are derived from a 125 MHz square wave that is phase locked to the 500 MHz ALS master oscillator and divided by four in the Timing module. The 3.0 GHz ( $6 * RF$ ) signal for the front-end phase detector is generated twice using two different techniques: the first

uses a Magnum Microwave (TLS22-06) x24 multiplier and phase locked loop (PLL) and the second uses a Herotek (GC125-188) step recovery diode whose rich spectral output is filtered by a 3.0 GHz band pass filter. Both methods produce spectrally clean and linear sine waves. The x 24 PLL output is a ready spare and a source for external mixer experiments. The 1.125 GHz carrier and the systems test 'fake beam' signal are also generated using the step diode recovery technique.

The 'fake beam' signal is a 3.0 GHz carrier modulated by the approximate synchrotron frequency (12 kHz) of the ALS and then is passed through an identical auxiliary comb filter. The resultant signal is a spectrally accurate reproduction of a longitudinally unstable beam with random coupled bunch motion. At the choice of the operator this signal can be switched to the input port of the front-end module thus providing a true calibration signal for the entire electronics chain from the front-end module to the power amplifier driving the kicker electrodes. This simple test along with alarm monitoring will allow technical personnel to quickly determine whether the electronics or the machine is at fault. System checkout is further enhanced by extensive front panel monitor points and the inclusion of a signal 'breakout panel' that collects all the signal monitor points from the other three modules into one 19" rack panel directly above the S.O chassis.

### 3.4 Timing module:

The timing module generates the fiducial (bucket zero trigger) for the down sampler module, the 500 MHz clock for both high speed digital modules, the 125 MHz source signal for the S.O. chassis, the re-synchronising pulse for the QPSK modulator, and complete temperature monitoring and alarm control for all the VXI modules and the S.O. chassis.

The temperature monitoring is a hardware only function that will automatically turn off the AC power to the VXI chassis if any of the sensors exceed pre-set limits. This feature is very crucial in preventing the burn-out of scarce and expensive high-speed memory chips in the downsampler and holdbuffer VXI modules.

## 4 RESULTS

The oscilloscope waveforms displayed in Figure 4 demonstrate the function of the Front-end RMS motion detector circuitry. The bottom waveform (trace 4) is an AM modulated sine wave injected into the Front-end module phase detector that mimics a slowly growing 'all mode' synchrotron bunch motion. Please note: The 27 ms periodic structure impressed on trace 4 is an artefact of the digital oscilloscope. The output of the RMS motion detector (trace 2) effectively tracks the growing synchrotron motion. At a pre-defined threshold set through the EPICS panel a comparator is tripped (trace 1). The comparator output which sends an alarm to the

EPICS panel can also be used to trigger the DSP farm to record a growing or runaway beam instability.

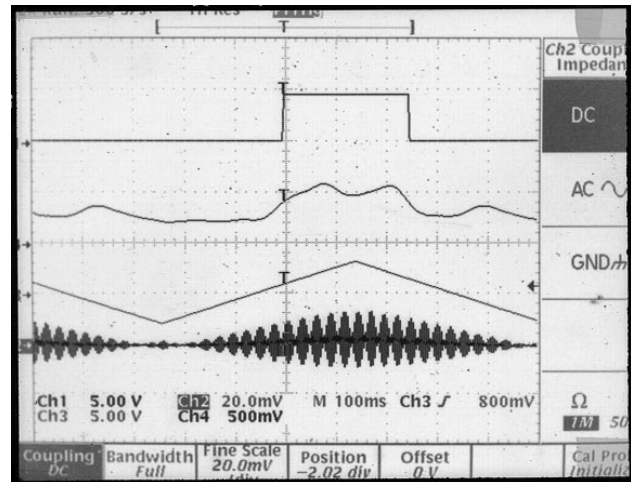


Figure 4. Hardware simulation of all mode beam instabilities (4), RMS motion detector output (2), comparator output (1), modulation envelope (3)

## 5 ACKNOWLEDGEMENTS

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