STATUS OF LONGITUDINAL FEEDBACK SYSTEM FOR THE PLS STORAGE RING*

Yujong Kim, J. Y. Huang, M. Kwon, I. S. Ko†, *PAL, POSTECH, Pohang 790-784, Korea*

Abstract

Originally, the Pohang Light Source (PLS) storage ring was designed to store the beam current up to 400 mA. But owing to the interactions between the HOMs of RF cavities and bunched beams which make the coupled bunch mode instabilities (CBMIs) such as dipole, quadrupole, and sextupole modes, the beam current can be stored up to 200 mA. So, to cure those CBMIs, a longitudinal feedback system (LFS) using parallel digital signal processors is necessary. After having considered the developing cost and the period, it was decided to install the LFS with electronics fabricated by SLAC and a pickup and a kicker designed by the PLS. At present, one aluminum kicker with 4 input/output ports and a nose cone is fabricated for the PLS longitudinal feedback system. With this LFS, it is possible to find the best operating condition for the temperatures of RF cavities and various fill patterns. The programmable LFS is useful for various beam diagnostics as well as for the cure of the CBMIs. Thus, it is also possible to measure the growth and damping rates of the instabilities, the HOM frequencies of RF cavities which generate the CBMIs, bunch-by-bunch current, bunch-by-bunch synchronous phase, and the longitudinal aliased impedances seen by the beam at revolution harmonics.

1 INTRODUCTION

To store the beam current up to 400 mA at 2.0 GeV and 250 mA at 2.5 GeV, the fourth RF cavity with 60 kW CW klystron amplifier was added in the PLS storage ring in 1996. But owing to HOMs of RF cavities that make the CBMIs, the stored beam current of the PLS storage ring is about 120 mA at 2.0 GeV. By analyzing the reverse signal of RF cavities and the sidebands of the BPM spectrum, it is found that the most dangerous HOMs of RF cavities are longitudinal TM_{011} (758 MHz) and TM_{013} (1707 MHz). To shift the frequencies of two dangerous HOMs, the cooling water temperature control system for the RF cavities was installed during 1997 Summer maintenance period. With the temperature control system, the stored beam current was increased from 120 mA to 200 mA. This means that all dangerous HOMs of the RF cavities can not be damped or avoided by the cooling system. Therefore, an active feedback system for curing the CBMIs is necessary for the PLS storage ring. There various types of LFS running at several accelerators such as PEP-II (SLAC), ALS (LBL), DAΦNE (LNF), KEKB (KEK), etc. In terms of the origin of impedance that generates the CBMIs, the feedback system can be classified into two kinds; the time domain system and the frequency domain system. The dangerous transverse or longitudinal HOMs of accelerating RF cavities can be cured by the time domain, bunch-by-bunch feedback system. The dangerous longitudinal fundamental mode of accelerating RF cavities and the dangerous transverse resistive wall impedance due to the beam pipe can be cured by the frequency domain feedback system. In case of the time domain feedback system, no pre-knowledge of the dangerous coupled modes is required while the pre-knowledge is required for the frequency domain feedback system. The LFS which have been developed by the collaboration of SLAC, LBL, LNF laboratories is a time domain, bunch-by-bunch feedback system which uses the programmable digital signal processing processors (DSPs). The typical LFS consists of a phase error pickup, digital signal processing units, and a kicker. For the PLS storage ring, one pickup which have already been installed for beam diagnostic purpose will be used as the phase error pickup, and one cavity which have been fabricated by the PLS and domestic manufacturer will be used as the LFS kicker. After having considered the developing cost and period, it is decided that the digital signal processing unit is purchased from SLAC [1].

2 LFS FOR THE PLS

The digital signal processing unit for the PLS LFS as shown in Fig. 1 consists of a system oscillator and a DSP farm with a VXI and two VME crates. A VXI controller, a timing module, a front end module, a down sampler module, a hold buffer module, and a back end module are housed in a VXI crate, and a VME controller, five DSP board modules, an interface module are housed in a VME crates.

2.1 Phase Error Detection

The longitudinal phase error detection is performed by a reserved BPM. The signals from the BPM are combined and then fed into the stripline comb generator where a coherent tone burst from the BPM signals is generated by a periodic microwave coupler circuit at six harmonic of RF frequency (3000 MHz). The phase error detection is performed by the double balanced mixer (DBM) where the signal from the comb generator is compared with 3000 MHz ($6 \times f_{RF}$) signal from the master oscillator phased locked to the ring. It is possible to obtain a phase processing range of $\pm 15^{\circ}$ at the f_{RF} with a resolution better than 0.5° by choosing the $6 \times f_{RF}$ as an operating frequency. A low pass filter is used to reduce the noise of DBM output.

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† Email : isko@postech.ac.kr

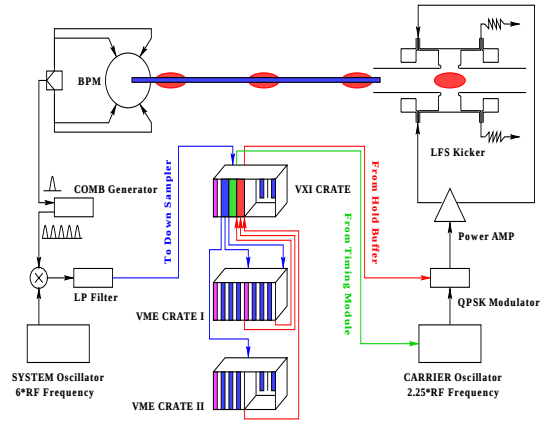

Figure 1: Block diagram of LFS for the PLS

Table 1: Parameters for the PLS LFS

Parameters	Value
RF frequency f_{RF}	500.082 MHz
Revolution frequency f_o	1.06855 MHz
Synchrotron frequency f_s	11.72 kHz
Ratio of f_o/f_s	90
Tap No of FIR algorithm N	≥ 6
Down sampling factor d	≤ 15
Bunch spacing for full filling	2 ns

2.2 *Down Sampling*

The detected phase error signals are digitized by an eight bit ADC converter at the bunch crossing rate (2 ns for fully filled buckets). To perform the longitudinal feedback, correction outputs must be calculated for every bunches and every turns in parallel, which means that a large number of DSPs will be needed. From the fact that the revolution frequency f_o of the PLS storage ring is ninety times greater than the synchrotron frequency f_s as summarized in Table 1, the calculating process can apply the Nyquist sampling theorem which states that it is possible to recover a signal from its samples if the signal is band-limited and the samples are taken at least at twice the highest frequency existing in the signal. Especially, in case of the sinusoid signal, it is possible to recover its amplitude and phase by taking only four samples per period. But, since the phase error oscillation (synchrotron oscillation) is not a perfect sinusoidal signal, six is selected as the number of taking samples per one synchrotron period for safety. In case of the PLS storage ring, taking six samples during one synchrotron period means that only the phase error values of every fifteenth turns will be used to calculate the correction output and the others (the phase error values from the first to the fourteenth turns) will be rejected in calculating the output. This process is called the down sampling whose the down sampling factor d is 90/6 =15. With this down sampling, the correction output can be calculated by sixty DSPs in parallel.

2.3 *DSP Farm and FIR Algorithms*

The DSP farm for the PLS LFS consists of two VME crates (three VME backplanes) and one VXI crate. The VME crates are fitted with VSB backplanes. The VME buses are used as the data buses while the VSB buses are used as the control paths. One VME crate has two VME backplanes where one Motorola MVME166 control processor and five DSP boards are housed. Each DSP board contains four 80 MHz AT&T 1610 DSPs. Each DSP chip has a 16 kB dual port memory (DPM) that can be accessible by the DSP and MVME166 control processor. The VXI crate having good electromagnetic shielding properties contains a National Instruments VXIcpu-030 control processor. After the longitudinal phase errors are detected and down sampled, the feedback correction output can be calculated by sixty DSPs in parallel which are housed at the fifteen DSP boards ($4 \times 15 = 60$) in three VME backplanes. To calculate the correction output, the DSPs use the N-taps finite impulse response (FIR) algorithm which is given by

$$y(t_n) = \sum_{k=0}^{N-1} h(k) \cdot \phi(t_{n-k}) \quad (1)$$

$$h(k) = 2^{G_s} \cdot G \cdot \sin(2\pi[k/N] + \varphi) \quad (2)$$

where $y(t_n)$ is the present correction output of the FIR filter, $h(k)$ is the programmable coefficient of the filter, $\phi(t_{n-k})$ is the phase error of previous turn as an input of the filter, G_s is the post multiply-accumulate shift gain of the filter, and G and φ are the gain and the phase of filter which can be used to choose the coefficient of FIR filter on EPICS operator interface. G = 0 means that feedback is off. In case of tap number $N = 6$, six sampled phase errors ($\phi(t_n) \sim \phi(t_{n-5})$) in one synchrotron period will be used to calculate a correction output $y(t_n)$. Therefore, DSPs will calculate one kicking output per every fifteen turns for a bunch. For 468 bunches, this calculation is performed by sixty DSPs in parallel according to lookup tables of the down sampler module.

2.4 *Hold Buffer*

The calculated correction outputs are sent to hold buffer with gigabit serial links. The hold buffer is a memory where the most recent kicking values are stored. Because of the down sampling, the most recent kicking values must be used to kick each bunch until a new kicking output is calculated by the DSPs. The output of the hold buffer drives a fast DAC converting at bunch crossing frequency and generates an analog signal which will be gone through the QPSK modulator, then be sent to the power amplifier.

2.5 *QPSK Modulator*

The central frequency of the LFS kicker can be given by

$$f_c = (p + 1/4) \cdot f_{RF} \quad (3)$$

or

$$f_c = (p + 3/4) \cdot f_{RF} \quad (4)$$

where p is any integer. When $p = 2$, $f_{RF} = 500$ MHz, and fully filled buckets, the central frequency f_c is given as 1125 MHz or 1375 MHz. f_c =1125 MHz (1375 MHz) means that the electromagnetic fields in the LFS kicker is changed 2.25 (2.75) times faster than the bunch crossing frequency (500 MHz). Therefore, to synchronize the electromagnetic fields in the LFS kicker with the bunch crossing, a phase shift must be needed at the bunch crossing frequency. For the f_c =1125 MHz (1375 MHz), $-\pi/2$ ($+\pi/2$) phase shift of the carrier oscillator will be needed to synchronize the kicking timing against the turning bunches. This process is called the quad phase shift key (QPSK) which enhances the kicking efficiency of the LFS kicker. The QPSKed signal is modulated in amplitude by the output signal of the hold buffer.

2.6 *Power Amplifier and LFS Kicker*

The selected power amplifier for the LFS kicker is a solid state type model AS0820-250R from MILMEGA. Its operation frequency range is 800 MHz $\sim$ 2000 MHz and the maximum output is 250 W. Its frequency response is tuned to operate two frequency ranges (for $p = 2$, 1000 MHz $\sim$ 1250 MHz and for $p = 3$, 1500 MHz $\sim$ 1750 MHz) with its best performance. This wide bandwidth and the frequency response tuning of the power amplifier make the upgrade of the LFS kicker easily. One aluminum single-ridged waveguide-overloaded cavity has been fabricated and tested to use it as a longitudinal bunch-by-bunch LFS kicker for the PLS storage ring. It has 4 input/output ports to obtain wide bandwidth ($\geq$ 250 MHz) and a nose cone is attached to increase the shunt impedance. Its measured bandwidth is about 344.4 MHz and its the maximum value of the shunt impedance is about 470 Ω. The phase error oscillation having phase deviation less than 10 mrad can be damped within 1 ms by this kicker without any amplifier saturation. By attaching the single ridge to a general waveguide and then adjusting the geometry, the frequencies of all dangerous HOMs can be increased higher than the cutoff frequency of the beam pipe ($\sim$ 2295 MHz) [2]. Therefore, the kicker is free from the dangerous HOMs which generate the CBMIs. The distribution of E field in the kicker which is an output of 3D HFSS code is shown in Fig. 2. Later, the kicker will be upgraded to improve the kicking efficiency by increasing the central frequency up to 1625 MHz.

2.7 *EPICS Operator Interface*

For the PLS LFS, the Experimental Physics and Industrial Control System (EPICS) is used for the control operator interface (OPI). The OPI has already been ported in a Sun sparc workstation. The setting of FIR algorithm, the diagnostic of LFS hardwares and data acquisition can be performed with the OPI.

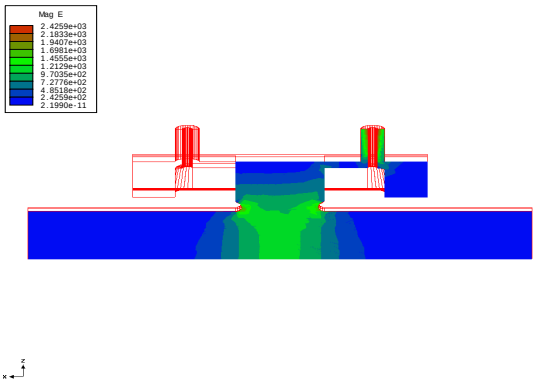

Figure 2: The distribution of E field in the LFS kicker

2.8 *Data Acquisition with LFS*

The feedback data is recorded in the dual port memory. With a code (gd_post), MATLAB compatible data file (gd.mat) can be obtained. With the MATLAB programmed codes, it is possible to obtain useful information such as the growth and damping rates of the instabilities, the HOM frequencies of RF cavities which generate the CBMIs, bunch-by-bunch current, bunch-by-bunch synchronous phase, and the longitudinal aliased impedances seen by the beam at revolution harmonics.

3 CURRENT STATUS

The pickup for the phase error detection has been installed and the power amplifier, the circulators, and all cables for the PLS LFS are ready. The LFS kicker has been fabricated and measured its properties. The kicker will be installed to the PLS storage ring in April 1999. If the electronics of the LFS is completed and delivered from SLAC, it will be possible for PLS to find the best operating condition for the temperatures of RF cavities and various fill patterns as well as damping the dangerous HOMs generating CBMIs. Also, the much narrower and higher intensity spectrum of U7 undulator can be obtained.

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