FAST SCR THYRATRON DRIVER*

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Abstract

As part of an improvement project on the linear accelerator at SLAC, it was necessary to replace the original thyratron trigger generator, which consisted of two chassis, two vacuum tubes, and a small thyratron. All solid-state, fast rise, and high voltage thyratron drivers, therefore, have been developed and built for the 244 klystron modulators. The rack mounted, single chassis driver employs a unique way to control and generate pulses through the use of an asymmetric SCR, a PFN, a fast pulse transformer, and a saturable reactor. The resulting output pulse is 2 kV peak into 50 Ω load with pulse duration of 1.5 μs FWHM at 180 Hz. The pulse risetime is less than 40 ns with less than 1 ns jitter. Various techniques are used to protect the SCR from being damaged by high voltage and current transients due to thyratron breakdowns. The end-of-line clipper (EOLC) detection circuit is also integrated into this chassis to interrupt the modulator triggering in the event a high percentage of line reflections occurred.

1 INTRODUCTION

The original thyratron driver had been designed and used since the beginning of SLAC modulator operations in the middle sixties. It could generate up to 5 kV at 1.5 μs pulses. However, it was large and heavy, required frequent intervention, and used PCB dielectric capacitors and unreliable thyratron and vacuum tubes. In 1992, a modulator reliability improvement project was established, and one phase was to replace these original drivers with solid-state trigger drivers utilizing modern components and packaging techniques. Besides meeting certain electrical and mechanical requirements, the new trigger generator reliability and manufacturing cost were of major concerns. Fast and extremely stable thyratron drivers had been designed and built for the kicker systems at SLAC [1-2], but they were quite expensive because of high part and assembly costs. This report describes the design and performance of an economical, reliable, fast, and high voltage thyratron driver.

2 DESIGN

A simplified circuit diagram of the driver is shown in figure 1. The basic pulse generating circuit consists of four essential components. They include a pulse transformer, a PFN, a thyristor, and a saturable reactor.

The pulse transformer T2 was commercially made by Stangenes Industries. It has a turns-ratio of 6 to 1 with a primary leakage inductance of only 100 nH.

The PFN, which comprises C2, C3, and L1, is a 1-section voltage-fed network that simulates an open-ended transmission line [3]. Its characteristic impedance, Zn, was designed to match with the load impedance reflected through the transformer. Lumped parameters were determined as follows.

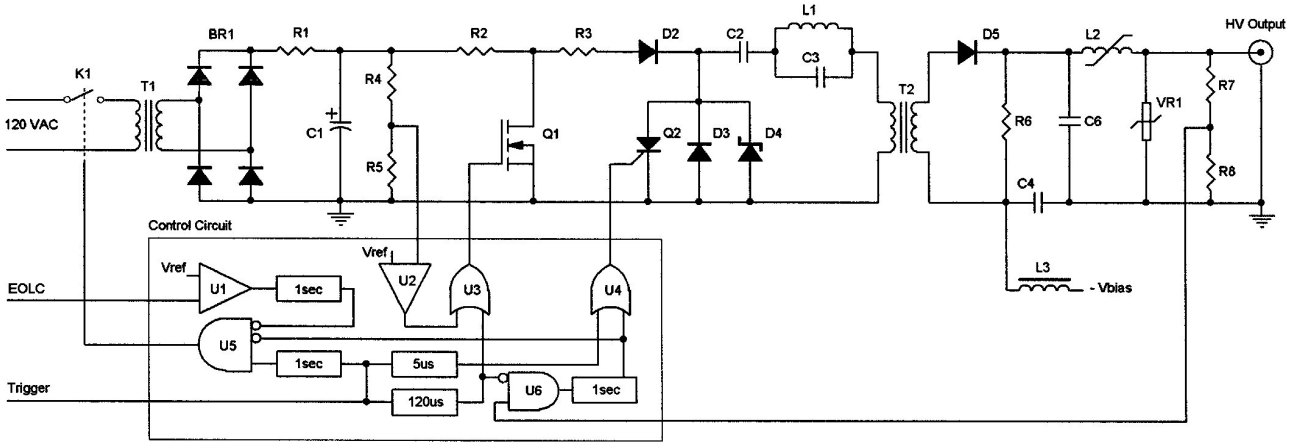

Fig. 1: Simplified circuit diagram.

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$C2 = Cn$
$C3 = Cn / 2$
$L1 = 2\,Ln / \pi^2$

where network capacitance Cn and inductance Ln were derived from the desired 50 Ω load impedance and 1.5 μs pulse duration.

$$Zn = Zload / N^2$$
$$= 50 / 6^2 \cong 1.4\ \Omega$$

$$Cn = \tau / 2\,Zn$$
$$= 1.5 \times 10^{-6} / 2 \times 1.4 \cong 0.6\ \mu F$$

$$Ln = Cn\,Zn^2$$
$$= 0.6 \times 10^{-6} \times 1.4^2 \cong 1.2\ \mu H$$

The thyristor Q2 is an asymmetric SCR from Mitel model ACR44. It is rated at 1200 V, 69 A RMS, and was particularly selected for its high di/dt rate of 2000 A/μs.

The saturable reactor L2 reduces the output risetime by a factor of three. It has a volt-second product of 225 Vμs, which was determined from the capacitor C6 charging voltage. Fair-Rite 43 NiZn material was used because of its relatively high magnetic flux density and low cost. An off-the-shelf ferrite bead P/N 2643540202 was then selected to fit in the available space on the PC board. The core o.d., i.d., and length h is 14.3 mm, 6.35 mm, and 13.8 mm respectively. From common transformer equations, the number of turns (N), the current required at saturation (Is), and the saturated inductance (Ls) were calculated as follows.

$$N = Epk\ ts / \Delta B\ Ac$$

where:

$\Delta B = Bs = 0.275$ T at $Hs = 795$ A/m
$Ac = h\,(od - id) / 2 = 55 \times 10^{-6}\ m^2$
$le = 2\pi\,(od + id) / 4 = 32 \times 10^{-3}$ m

$$N = 225 \times 10^{-6} / 0.275 \times 55 \times 10^{-6} \cong 14\ \text{Turns}$$

and:

$$Is = Hs\ le / N$$
$$= 795 \times 32 \times 10^{-3} / 14$$
$$= 1.8\ A \approx 5\%\ \text{load current}$$

and:

$$Ls = \mu\ N^2\ Ac / le$$

where:

$$\mu = \mu 0\ \mu sat = 1.256 \times 10^{-6} \times 2 = 2.5 \times 10^{-6}\ H/m$$

$$Ls = 2.5 \times 10^{-6} \times 14^2 \times 55 \times 10^{-6} / 32 \times 10^{-3} = 0.85\ \mu H$$

The following is brief description of the circuit operation.

Low-level voltages simultaneously trigger three retriggerable monostables of 1 second, 120 μs, and 5 μs wide pulses. The first pulse of 1 second, which is gated by U5, switches on solid-state relay K1 for the high voltage power supply. Subsequent pulses of 5 μs and 120 μs are then used to trigger SCR Q2 and MOSFET Q1. While the MOSFET serves to turn off the SCR by shunting anode current, it is also used as a switching element to regulate the PFN charging voltage by way of error amplifier U2. Figure 2 shows waveforms of Q1 switching regulation and PFN charging voltages. Comparator U1 monitors peak and average currents of the modulator EOLC, and turns off the power supply when these currents exceed a predetermined value.

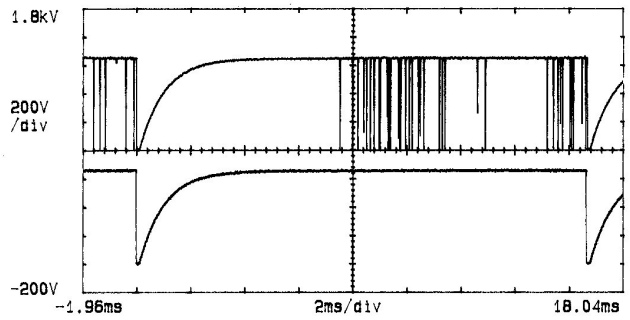

Fig. 2: Typical MOSFET and PFN charging voltages.

When the AC line supplies 120 V to power transformer T1, the secondary voltage is rectified and filtered and shunt-regulated to ≈ 640 VDC by BR1, C1, R1, R2, and Q1. The PFN is resistively charged at the same time by the regulated voltage via R2, R3, and D2. Once Q2 is turned on, the PFN discharges one-half of its voltage into the primary of pulse transformer T2. The secondary voltage is then applied to saturable reactor L2 which, when saturated, sharpens the output voltage rise. The resulting pulse output of 2 kV peak into 50 Ω resistive load (4 kV open circuit) at 1.4 μs FWHM is shown in figure 3.

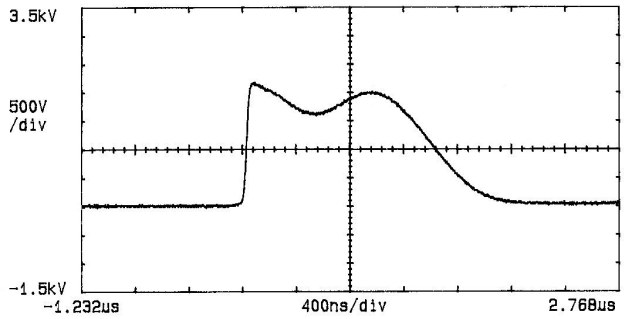

Fig. 3: Output voltage waveform.

Figure 4 shows the effect of saturable reactor on output risetime. A 1-stage pulse sharpener shortens the voltage rise as shown from 119 ns (10 – 90%) to 36 ns. A second stage, which has been tested with CMD-5005 core but not been implemented on this chassis, further reduces the risetime to 12 ns.

Thyratron breakdowns as a result of either misadjusted reservoir voltages or aging thyratrons [4] can generate destructive transient voltage and current for the SCR; therefore, several SCR protection devices are necessary.

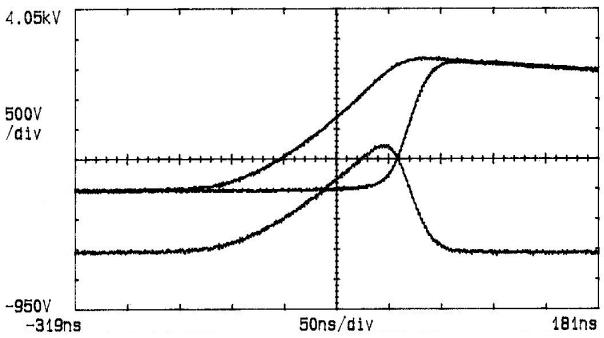

Fig. 4: Voltage rises before and after 1-stage sharpener, and saturating reactor voltage.

Fast turn-on diode D3 and transzorb D4 are used to limit the anode reverse and forward blocking voltages. On the output side, VR1, which consists of two series GE metal-oxide varistors rated 180 joules at 1.2 kV each, clamps down transient voltages while diode D5 blocks the reverse current. To further reduce the chance of an SCR failure by a soft turn-on due to high ground potentials, which can sometimes build up on the gate after a rapid set of thyratron fire-throughs, an active feedback scheme is employed. A portion of the output voltage is gated through U6 with the 120 μs command trigger pulse. A thyratron arc that randomly occurs outside this timing window would immediately turn on the SCR and shut off the high voltage supply for a period of 1 second before returning to normal operation.

For ease of manufacture and low assembling cost, all connectors and electrical components were mounted on a single 0.093 inches thick PC board. One exception was the output HN connector that must be mounted directly on the chassis for mechanical strength. The driver was simply constructed by fitting together the PC board, front, rear, and side panels of a standard 19 x 5.25 x 8 inches rackmount chassis. Figure 5 shows a photograph of the complete trigger generator PC board.

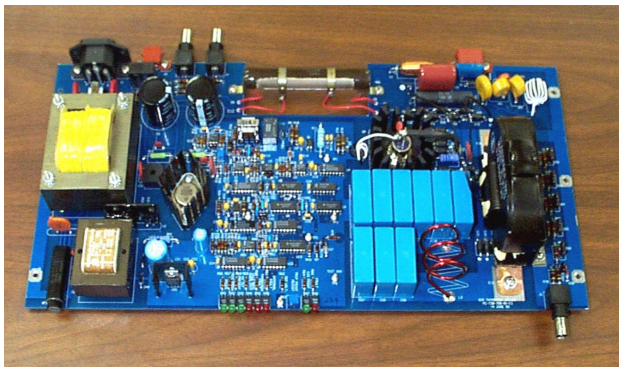

Fig. 5: Photograph of the complete driver on PC board.

3 PERFORMANCE

Jitter and long-term timing drift were measured with SR-620 Universal Time Interval Counter. The test conducted at 120 Hz with a sample size of 5000 shots. A typical result of jitter distribution is shown in figure 6. The graph displays a peak-to-peak jitter of 320 ps with standard deviation or RMS jitter of 72 ps. Throughput delay, defined as the timing difference (on rising edges at half maximum) between the trigger input and the pulsed output, is 580 ns. A 24-hrs run test at 20°C temperature excursion resulted in a timing drift of less than 3 ns.

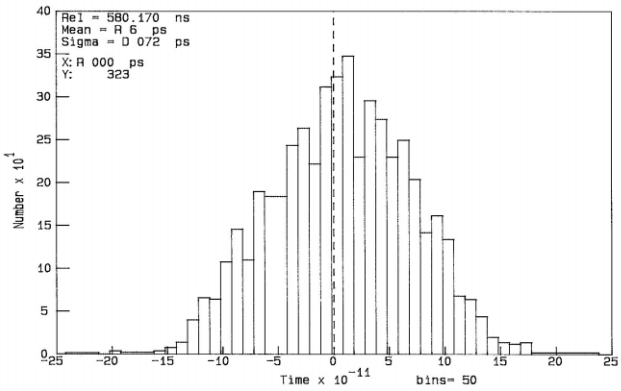

Fig. 6: Histogram of jitter distribution.

The mean time to failure (MTTF) rate, which was calculated based on actual data collected over several years, is 195,000 hours. More detailed discussions of the modulator reliability can be found in the report [5].

4 CONCLUSION

New thyratron drivers for the 244 SLAC klystron modulators have been economically built and operated since 1994. In several years of operation, these drivers have contributed to the modulator stability and proven to be very reliable.

5 ACKNOWLEDGMENTS

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6 REFERENCES

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