DIGITAL RECEIVERS OFFER NEW SOLUTIONS FOR BEAM INSTRUMENTATION

R. Ursic, Instrumentation Technologies, Srebrnicev Trg 4a, 5250 Solkan, Slovenia
R. De Monte, Sincrotrone Trieste

Abstract

Digital receivers revolutionize today's telecommunication industry. In this article we examine the features, the applications and the opportunities of this new and promising technology from the beam instrumentation point of view.

1 INTRODUCTION

Since the invention of the superheterodyne receiver, radio architecture has remained remarkably unchanged. While it is true that development has not stood still - increasing integration, ever more sophisticated devices, and the use of digital circuitry to implement baseband functions are just some examples of technological advancements - it is also true, that none of these developments can be said to have revolutionized the original concept. It seems however, that such a revolution may already be in progress, in the guise of the so-called digital receivers or software radio. The purpose of a digital receiver is similar to that of his analog counterpart: to downconvert, filter and recover any analog signal, such as those signals with amplitude, frequency or any other kind of modulation. Its main advantage lies in its programmability which means that new functions, features and upgrades to the system do not necessitate hardware re-design, but rather the writing and loading of software code.

There are clearly many advantages of using digital receivers in telecommunications. The economy of scale of such a huge market and the unrelenting search for the holy grail of all things cheaper, faster and more versatile, make digital receivers also an attractive option for particle accelerator beam instrumentation.

2 THE DIGITAL RECEIVER CONCEPT

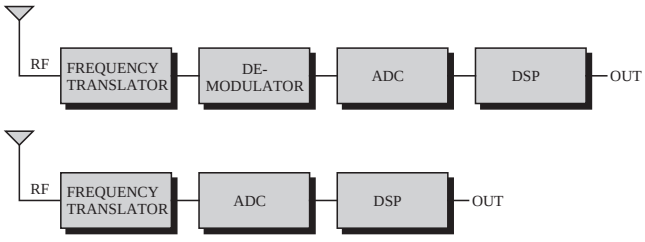

Figure 1: Block diagram of the analog (top) and the digital receiver (bottom) counterparts.

3 TECHNOLOGY DRIVERS

3.1 Analog to Digital Converter

Some of the key parameters in the specification of an analog-to-digital converter (ADC) for intermediate frequency (IF) digitization are: sampling rate, bandwidth, signal-to-noise ratio, and dynamic range. Much research and development is being carried out on faster ADCs, with wider bandwidths and larger dynamic ranges. Companies such as Harris Semiconductor and Analog Devices are producing the current state-of-the-art devices. An example of a low cost state of the art ADC for digital receiver applications is the AD9042 from Analog Devices. It is a 12 bit ADC, has 41 MHz maximum sampling rate and 100 MHz analog bandwidth.

3.2 Digital Signal Processing

With the wideband IF signal successfully digitized, at a reasonable sample rate, the next stage is the processing. It would be convenient at this point to simply transfer the digital data to one or more digital signal processor (DSP) chips, and implement all remaining functions in software. However, even a cursory look at the processing demands of digital receivers makes it apparent that this operation is not straightforward. The total processing requirements in such a receiver may add up to more than 10 GFLOPS (giga floating point operations per second). Clearly, to implement all the radio functions using DSP alone would require an impractical number of chips. The answer? A hybrid approach incorporating specialized digital hardware, a digital downconverter (DDC), which performs specific tasks (downconversion, filtering, sample-rate reduction, demodulation, amplification) to reduce considerably the load supported by the DSP.

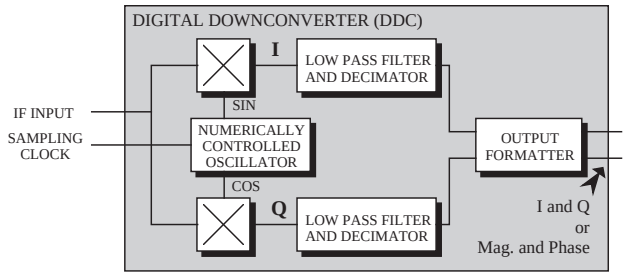

Figure 2: Functional block diagram of a DDC integrated circuit.

Companies such as Analog Devices, Graychip and Harris have developed a number of DDCs. Devices such as these are essential components of current digital receivers, and will be until DSP chips are developed that possess the

necessary horsepower to handle far higher bit rates than present technology allows.

3.3 RF Front End

The focus so far in this article has been on the digital (and analog/digital interface) hardware necessary for digital receiver implementation. However, such a receiver design also has implications for the RF front end circuitry, depending on the particular approach taken, and also depending on the particular application. In the RF front end, special filters, gain control schemes and very linear amplifiers (to provide a large dynamic range) may be required.

4. FEATURES AND PERFORMANCE OF DIGITAL RECEIVERS

In this paragraph we examine some of the features and performance of digital receivers that are of particular interest to beam instrumentation.

4.1 Linearity

Linearity of a conventional analog receiver is defined by the most nonlinear element in the processing chain, which is usually the analog demodulator. Digital receiver on the other hand implements digital demodulation, which shifts the source of non-linearity either to the RF front end or the ADC. With a careful RF front end design we can minimize non-linearity effects by driving all the active components well below the 1 dB compression point. As an example we can examine linearity characteristics of the AD9042 ADC:

Differential non-linearity	±0.3 LSB or	$\pm 7.3\ 10^{-5}$ FS
Integral non-linearity	±0.75 LSB or	$\pm 1.8\ 10^{-4}$ FS

A possibility to implement a simplified gain control scheme is just one of the possibilities offered by the excellent linearity of ADCs; one can easily imagine having a fixed gain RF front end for a system with a 40 dB dynamic range.

4.2 Temperature Stability

The AD9042 also offers excellent temperature stability. Its gain drift is guaranteed to -50 ppm/°C. To verify this parameter we have setup a measurement, where we applied two signals of approximately same amplitude to two AD9042 converters. The two ADCs resided on a single VME board, one on the top and the other on the bottom. The measurements were take over a period of 16 hours, the ambient temperature changed for 5 °C and the temperature of the two converters tracked each other within app. 1 °C.

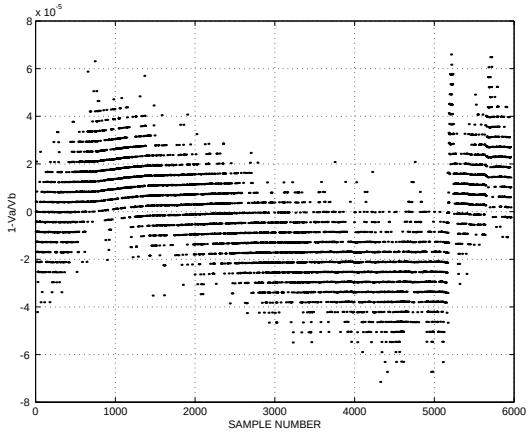

Figure 3: Deviation of the ratio between the readings from two AD9042 ADCs. Va and Vb are readings from the two ADCs respectively.

4.3 Processing Gain

Processing gain is the improvement in the signal-to-noise ratio gained through the oversampling and digital filtering. It is the ratio of the passband to the Nyquist bandwidth expressed in dB. An important consequence of the processing gain is the effective increase in resolution. For example, if an IF signal is being sampled and digitized at 40 MHz (Nyquist bandwidth = 20 MHz) and we set the digital filter to 20 kHz the processing gain would be -10 x log(0.02 MHz/20 MHz) or 30 dB. In other word we gain 5 bits of resolution.

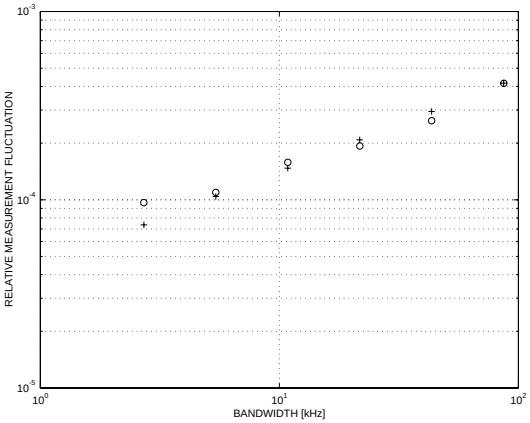

Figure 4: Processing gain shows up as decrease in measurement fluctuation. The graph shows measured (o) and predicted (+) measurement fluctuation for different bandwidth settings. The measurements were done with AD9042 ADC and GC1011 DDC from Graychip. The GC1011A is an all digital downconverter which can extract narrow band signals from wide band digitized sources.

4.4 Undersampling

Undersampling is a very attractive technique that has two important advantages. First, it drastically reduces the sample rate requirements. Second, it downconverts (aliases) a bandlimited IF signal close to the baseband.

The theory underlying the undersampling technique is that the Nyquist's theorem is met with respect to bandwidth, rather than the absolute frequency of a bandlimited IF signal. In other words sampling must occur at a rate of twice the bandwidth of the desired signal, resulting in the band of interest being aliased down to a frequency band close to dc. The result of the AD9042 undersampling performance test is shown in figure 5.

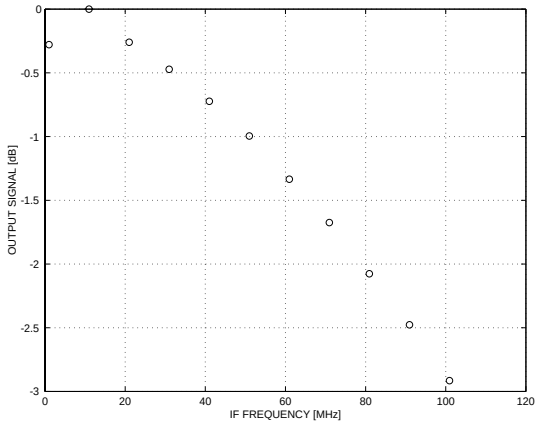

Figure 5: We cascaded an AD9042 ADC and a GC1011 DDC tuned to 1 MHz. Sampling frequency = 10 MHz. The graph above shows amplitude of the output signal for different input IF frequencies (1 MHz, 11 MHz, 21 MHz, up to 101 MHz) aliased to 1 MHz.

4.5 Multicarrier Receiver

High sampling frequencies delivered by today's state of the art ADCs allow a wide spectral input signal to be transferred to the DDC. This wide-band approach also offers a multi-channel advantage over a standard narrowband approach. The main advantage is that the RF front end does not need to be reduplicated in case we want to recover multiple carriers. We need only one DDC per channel or, in case the real time response is not required, we can use time multiplexing of a single DDC to recover multiple carriers.

5 SOME IMPLEMENTATION EXAMPLES AND OPPORTUNITIES

The new BPM system under development at the Paul Scherrer Institute for the Swiss Light Source implements digital receivers to measure the amplitude of individual pick-up button signals [1]. The digital receiver is built around Harris HSP50214 DDC integrated circuit interfacing to Analog Devices SHARC DSP. Set to low-bandwidth (10 kHz), the system offers high stability, accuracy and resolution. Set to wide-bandwidth (600 kHz), the system supports turn-by-turn and tune measurements.

An other opportunity for digital receiver technology are lock-in amplifiers. They are used to detect and measure very small AC signals up to approximately 100 kHz. They use a technique known as phase-sensitive detection to single out the component of the signal at a specific reference frequency and phase. Digital lock-in amplifiers, which internal architecture resembles that of a digital receiver, have been successfully used for beam diagnostics in the past [2], [3]. Digital receivers based on fast ADCs and DDC integrated circuits look as a promising technology for building new generation lock-in amplifiers with wide frequency range spanning couple of tens of MHz.

The technique of controlling the in-phase (I) and the quadrature (Q) components is gaining in popularity with respect to standard amplitude (A) and phase (F) control loop approach in the field of low level RF control. Stability, excellent phase detection performance and programmability make digital receiver a promising technology for this application too.

6. CONCLUSION

Digital receivers are an exciting new technology that paves the ground for the development of new and innovative low-cost and high-performance beam instrumentation systems. The digital receiver building blocks are primarily designed for and used in the telecommunication industry. However, the few features and tests presented in this paper demonstrate that such components offer excellent building blocks for beam instrumentation devices. An other advantage that we can capitalize on is the economy of scale in the telecommunication industry that continuously pushes the prices down.

7 REFERENCES

[1] M.Dehler et.al, " SLS Storage Ring BPM System", paper presented at this conference

[2] B. Podobedov and R. Siemann, "New aparatus for precise synchronous phase shift measurements in storage rings", Physical review special topics - accelerators and beams, Volume 1, 072801

[3] Rok Ursic et.al, "1 nA Beam Position monitoring system", Proceedings of the 1997 Particle Accelerator Conference, Vancouver, Canada