CONTROL AND TIMING SYSTEM DESIGN OF CPHS *

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Abstract

The Compact Pulsed Hadron Source (CPHS) in Tsinghua University is designed as a university based comprehensive hadron research and application platform. This paper describes the control and timing system of CPHS.

INTRODUCTION

The project of CPHS in Tsinghua University consists of an accelerator front-end—a high-intensity ion source, a 3 MeV radiofrequency quadrupole linac (RFQ), and a 13 MeV drift-tube linac (DTL), a neutron target station—a beryllium target with solid methane and room-temperature water moderators/reflector, and experimental stations for neutron imaging/radiography, small-angle scattering, and proton irradiation. [1,2]

The control system of CPHS consists of an EPICS (Experimental Physics and Industrial Control System) based distributed run-time database and control system, a timing and event distribution system, and a digital low level RF control system.

The timing and event distribution system defines the global system time frame as well as specific events that trigger local devices by an event generator and receiver framework, so that the time delay of each event could be controlled in 10ns resolution, and the timing jitter of trigger signal is below 0.1ns. The hard-real-time machine protection system is also integrated in the event system so that a fault event could be responded within 50 micro-seconds. Field control signals such as water temperature, vacuum level, magnetic current, beam diagnostics, and low level RF (LLRF) phase and amplitude are monitored and controlled via the EPICS database through Ethernet.

EPICS BASED CONTROL SYSTEM

Control System General Layout

As shown in Fig 1, the EPICS control system uses several input/output controllers (IOC) to manage local process variables and establish a distributed database. The IOCs are running Linux/RTEMS kernels with device support of different local bus interfaces (serial, GPIB, stepper motor, DAQ modules, etc), communicating with local instruments monitoring and controlling water temperature, power supply, vacuum status, and LLRF status. All EPICS records are accessible from control room via Ethernet by Channel Access protocol, and are managed through Operator Interfaces (OPI) for monitoring, data logging, alarm handling, and some interlocking control. The application server and development server are responsible of providing dhcpd/bootp/nfs services for net-booting IOCs and maintaining IOC kernels, IOC applications, bootup scripts and EPICS records.

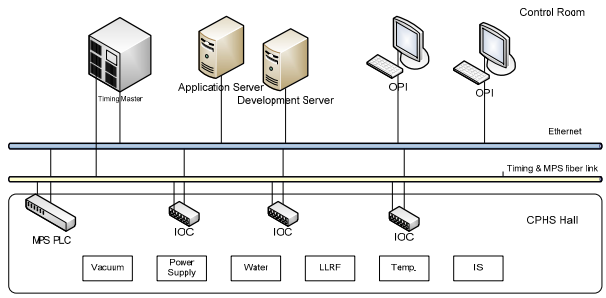

Figure 1: EPICS control system for CPHS

TIMING AND EVENT DISTRIBUTION SYSTEM

Timing System General Layout

CPHS timing events are generated, encoded and distributed through optic fiber at 108.3MHz rate (325MHz divided by 3), and then decoded by different local receivers. (Fig 3.)

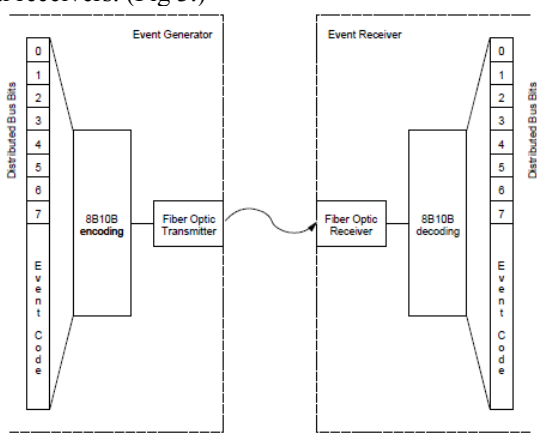

Figure 2: Event frame [3]

The event generator (EVG) is responsible of creating and sending out timing events to an array of event receivers through a fanout module. The event transfer rate is derived from the linac RF master frequency at 325MHz. The EVG is also capable of synchronizing to the AC line at 50Hz and phase delay to adjust the triggering position relative to the main voltage phase.

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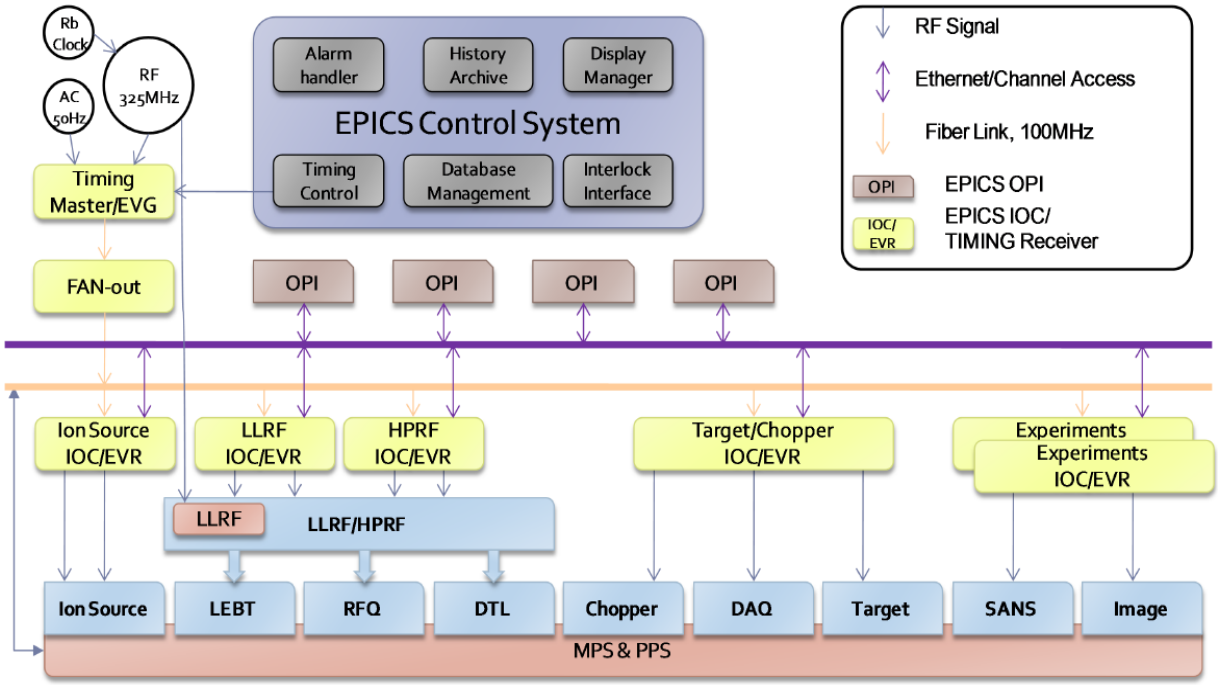

Figure 3: Framework of CPHS event distribution system

EVG accepts input from external RF clock (325MHz) with no PLL, while each EVR has a PLL tuned with ±20ppm precision to the master clock.

The event receiver (EVR) is responsible of receiving and decoding event frames. A global time stamp is also distributed as 32-bit unsigned integer to EVRs. The EVR includes a prescaler and delay counter to adjust local trigger pulse delay. The controller of EVR is integrated with an EPICS real-time IOC so that event encoder, sequence, local delay, local trigger frequency are able to be managed through any EPICS OPI.

Events are encoded and queued by EVG, and then distributed by a fanout module to local EVRs through fibre link as event frames which consists of a 16-bit frame: eight bit event code and eight bits of distributed bus bits as shown in Fig 2. The event bit rate is 20 times event code rate, which is 2.16GHz in our case.

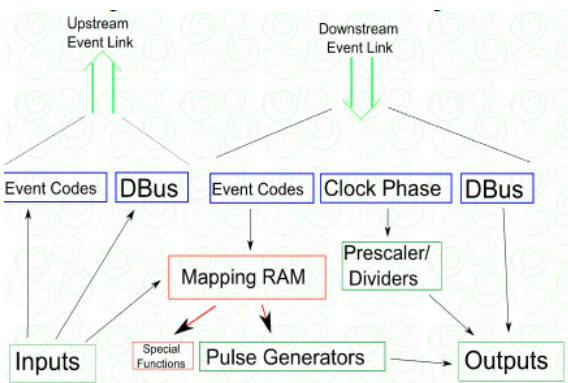

Figure 4: Downstream/Upstream event link

Besides the downstream event link, there is also an upstream from EVR to EVG with the same frame bit. This mechanism could be used as the interlock scheme for machine protection systems. (Fig 4.)

Hardware

The EVG and EVR are selected using commercial products from Microresearch Finland, which was conceptually based on event systems of ANL APS and Swiss Light Source. The hardware module is PXI compatible, and the firmware is configured with modular register mapping.

EVG and EVR are installed in separate PXI chassis with embedded controllers from National Instruments. The controllers are connected to the EPICS control network for remote access. A 12 way fanout module is used to distribute fibre signals from EVG to multiple EVRs.

The picture of EVG and EVR module is shown as Fig 5.

Software and EPICS support

There already are EPICS support for MRF hardware in use at SLS, SLAC, Diamond, etc, but the support of modular regster mapping cPCI hardware is just under development by the project mrfioc2[5,6], which also follows the regime of devLib-pci, the operating system independent device support of EPICS.[7]

Every EVG and EVR module has a separate controller running Linux or RTEMS 4.9.4 with an EPICS application. The controller is configured to be net-booted from the application server with gPXE[4] boot-loader.

The EPICS application is built on EPICS base 3.4.11 with mrfioc2 support, which containing the common devPCI driver module, MRF common PCI API, EVG/EVR device support module, and a set of EPICS records with interface of Channel Access protocol.

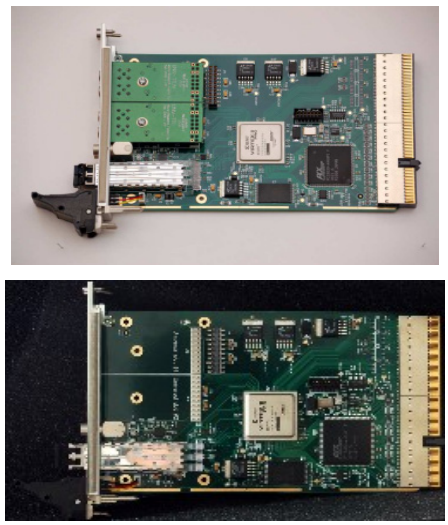

Figure 5: Picture of PXI event generator/receiver.

CONCLUSION

The prototype of CPHS control and timing system is developed with EPICS support. The timing system is built based on MRF event distribution devices, and the OS-independent EPICS device support module for EVG and EVR are tested on Linux 2.6 and RTEMS 4.9.4.

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