DIGITAL PULSE PROCESSING TECHNIQUES FOR HIGH RESOLUTION AMPLITUDE MEASUREMENT OF RADIATION DETECTOR

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Abstract

The digital pulse processing techniques for high resolution amplitude measurement of radiation detector pulse is an effective replacement of expensive and bulky analog processing as the digital domain offers higher channel density and at the same time it is cheaper. We have demonstrated a prototype digital setup with high-speed sampling ADC with sampling frequency of 80-125 MHz followed by series of IIR filters for pulse shaping in a trigger-less acquisition mode. The IIR filters, peak detection algorithm and the data write-out logic was written on VHDL and implemented on FPGA. We used CAMAC as the read out platform. In conjunction with the full hardware implementation we also used a mixed-platform with VME digitizer card with raw-sample read out using C code. The rationale behind this mixed platform is to test out various filter algorithms quickly on C and also to benchmark the performance of the chip level ADCs against the standard commercial digitizer in terms of noise or resolution. The paper describes implementation of both the methods with performance obtained in both the methods.

INTRODUCTION

In digital pulse processing technique, detector or preamplifier output signals are directly digitized and processed to extract quantities of interest. Our concern is to detect energy of the particle, which is proportional to amplitude of preamplifier output pulse. Traditional analog electronics is here replaced by programmable digital filters. Most of the typical processing features, e.g., pole-zero cancellation, baseline restoration, and shaping are digitally implemented and optimized. Costly peak sensing ADC is replaced by low cost fast ADC. It has been suggested that, typical fast AD converter should have resolution of 10–12 effective number of bits and sampling frequency 50–200 MSPS, for accurate energy measurement [1, 2]. Two digital pulse processing techniques - software based and hardware based, using such ADCs, are proposed and demonstrated for high resolution amplitude measurement of radiation detector pulse.

SOFTWARE BASED PULSE PROCESSING

In first technique of digital pulse processing, digital filters and peak detection algorithm was designed and implemented at software level. It is easy to start with such flexible system as various pulse processing features like pulse shape, shaping time, pole-zero compensation can be easily modified and tested by varying the parameters for various detector systems and various ADCs. Figure 1 shows the block diagram of software based pulse processing system.

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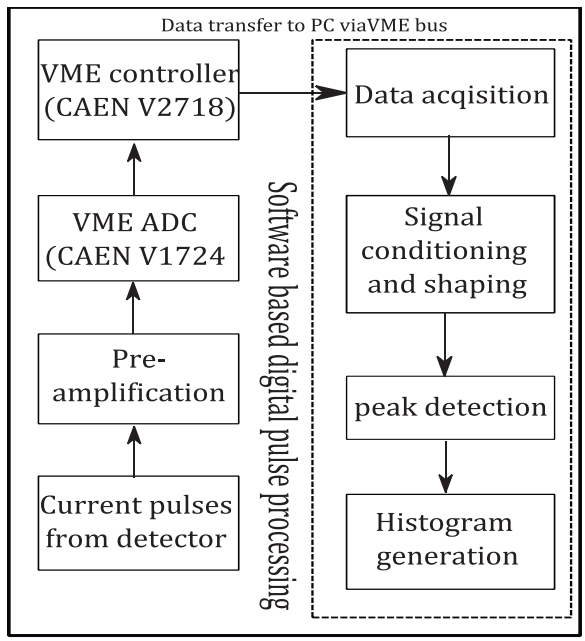

Figure 1: Software based pulse processing system.

Data is sampled by a 14 bit 100 MSPS VME ADC. The data stream is continuously written in a circular memory buffer and read via VME. The major problem of software based system is that the amount of data to readout is extremely high. It is not possible to sustain a continuous acquisition and transfer all the data to the computers. Therefore the data is acquired through block transfer mode at the cost of loss of many events. Fragmented data is discarded at the beginning and end of the block. All pulse processing features are designed at software level using 'C' programming. Codes are written to implement digital filters for CR-RC shaping of pulse, along with pole-zero compensation, whose difference equation is represented by equation 1.

$$\boldsymbol{y(n) = b_1 \times y(n-1) + b_2 \times y(n-2) + a_0 \times x(n) + a_1 \times x(n-1) + a_2 \times x(n-2)} \quad (1)$$

Shaping time of filter is decided by coefficients b_1, b_2 and pole-zero compensation depends on a_0, a_1 and a_2 for a certain sampling frequency.

Figure 2(a) shows two overlapped preamplifier pulses at the input of digital CR-RC filter and 2(b) shows clearly resolved pulses with better SNR at the output of filter. A trigger less peak detection logic is developed to measure amplitude of filtered pulse. The peak detector logic is one

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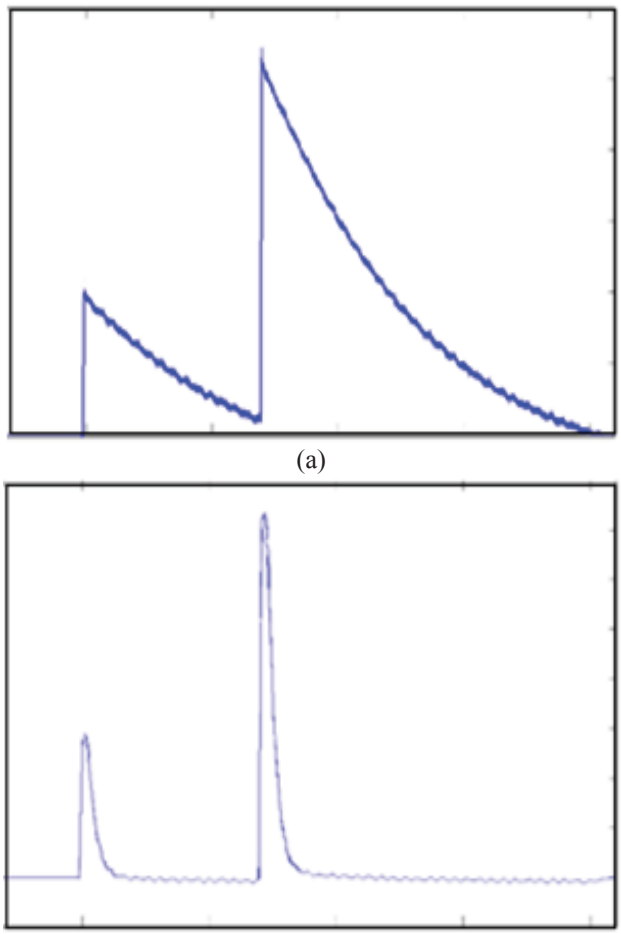
of the most critical parts of this program, since in involves eliminating the jitter noise which present in almost every natural system. After detecting the peak amplitude of filtered pulse, it is plotted on histogram to analyse energy information of particle.



(a) (b)

Figure 2: Input and output of digital CR-RC filter.

HARDWARE BASED PULSE PROCESSING USING FPGA

In this scheme all of the pulse processing blocks used in software based system is translated into a hardware system for real time implementation. This system is having advantage of zero dead time and no loss of events.

A continuous running, trigger-less, digital system is optimally designed and implemented at hardware level to perform typical processing tasks i.e. automatic pole-zero cancellation, CR-RC shaping and peak detection. Spectroscopy performances are achieved using low-cost and relatively low-resolution (12-bit) AD converters at high sampling frequency (80-100MSPS). It is not possible to run filter loop within 10-12 ns with the digital signal processors, therefore we choose FPGA to implement the design in the hardware level itself. For current implementation, XC4VLX25 Virtex 4 FPGA [3] has been chosen as target device. Figure 3 shows block diagram of this system.

Preamplifier pulse is sampled using fast digitizer. This sampled data is then transferred to FPGA for digital pulse processing. VHDL codes have been written to implement automatic detection of fall time, digital IIR filter for pole-zero compensation and CR-RC shaping (represented by Equation 1) and trigger less peak detection. These codes are first simulated successfully and then implemented on FPGA. Output of peak detection is read by CAMAC based data acquisition system and plotted on histogram for further energy analysis.

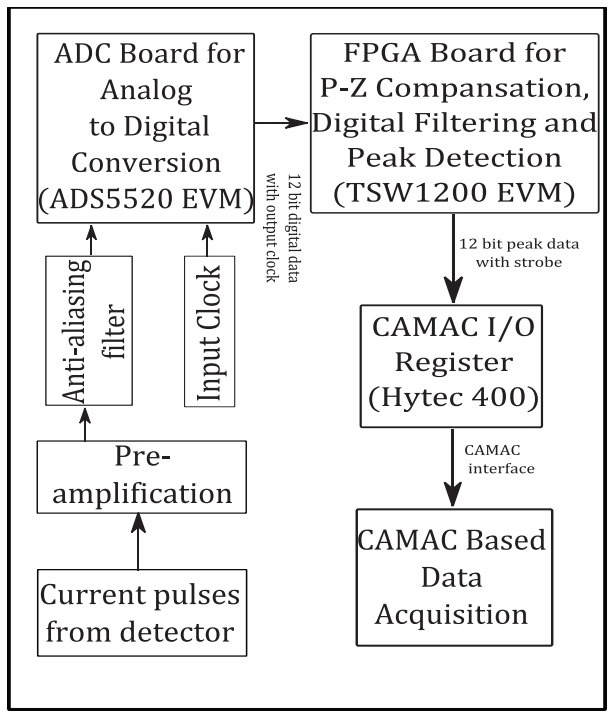


Figure 3: Hardware based pulse processing system.

EXPERIMENTAL RESULTS AND ANALYSIS

Performance of the digital systems is tested with, first data from precision pulsar and then from actual radioactive sources using semiconductor detectors. In order to measure the resolution of proposed digital systems, HPGe detector (resolution nearly equal to 2 KeV) is used with a source of ^{60}Co. Performances of both the systems are compared with traditional analog spectroscopy system.

Figure 4(a) shows spectrum of ^{60}Co source, obtained from traditional analog spectroscopy amplifier, using CAMAC based 13 bit peak sensing ADC (Ortec 413). Resolution of this system at spectral line 1332 KeV is **0.192%**. Figures 4(b) and 4(c) shows the spectrum obtained from software and hardware based digital pulse processing system respectively. A linear amplifier with no pulse processing feature is used with both the systems to enhance the preamplifier output signal. Resolution obtained with VME ADC based digital system was **0.532%** and that with FPGA based system was **0.578%**.

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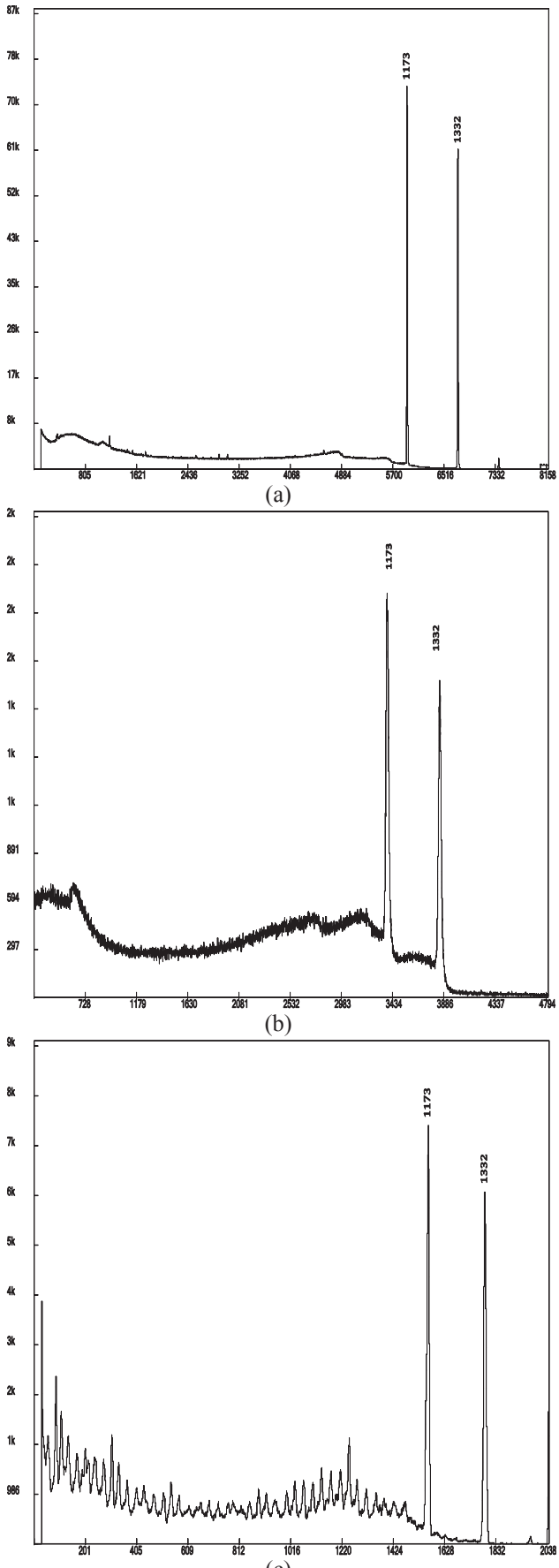

Figure 4: Spectrum of ^{60}Co.

FUTURE SCOPE

It is planned to develop the whole digital pulse processing system including anti aliasing filter, fast digitizer and various digital filters implemented on FPGA on a single board, in the near future. This will help to remove the distortion in the clock and other signal because of wires used to interface various devices. Also using proper design and shielding, noise contributed by ground can be reduced to result better resolution. The board is planned to design for multi-channel system by optimizing the resources available in FPGA.

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