THE NEW WHITE RABBIT BASED TIMING SYSTEM FOR THE FAIR FACILITY

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Abstract

A new timestamp and event distribution system for the upcoming FAIR facility is being developed at GSI. This timing system is based on White Rabbit (WR), which is a fully deterministic Ethernet-based network for clock and time distribution. WR is developed by CERN, GSI and other institutes as well as partners from industry based on Synchronous Ethernet and PTP [1].

The main tasks of the General Machine Timing (GMT) system are time synchronization of more than 2000 nodes with nanosecond accuracy, distribution of timing messages and subsequent generation of real-time actions (interrupts, digital signals...) by the nodes of the timing system. This allows precise real-time control of the accelerator equipment according to the beam production schedule. Furthermore the timing system must support other accelerator systems like post-mortem [2] and interlock [3]. It also provides interfaces between the accelerator control system and experiments at FAIR.

INTRODUCTION

The GMT triggers and synchronizes accelerator equipment, timed according to the accelerator cycles [4]. Cycle lengths range from 20 ms (present UNILAC), several seconds (synchrotrons SIS18 and SIS100/300) to several hours (storage rings). An important concept of the accelerator control system is the one of the so called *beam production chain*, which describes the production of a beam from an ion source through the accelerators to a target. Properties of such a beam production chain include the ion type (from protons to uranium), energy, intensity, focus and emittance at the final destination and other parameters. This is mapped to the GMT, which has an integral view on the tightly synchronized accelerators and beam transfer sections. The GMT must take into account the execution of several beam production chains in the accelerator complex at the same time. For each part of the machine, switching between different beam production chains will be possible between cycles, which implies a high degree of true parallel operation.

For all components, set values or ramp data for the different beam production chains are preloaded in the Front-End Controllers (FECs). This is done by the control system via its general purpose network. The task of the GMT is to trigger and synchronize the FECs in real-time via *timing events*, which carry additional information like machine ID or event numbers. After parameterization of the facility by the top and middle layer of the control system, it is finally the GMT which autonomously operates the accelerator complex in real-time.

Besides the GMT, the so-called Bunch phase Timing System (BuTiS) serves as a campus-wide distribution system for clock signals. BuTiS is focussed at synchronizing the radio-frequency systems of the accelerator and provides distributed and synchronized clock signals with a precision in the low picoseconds and jitter in the low femtoseconds range [5].

REQUIREMENTS

The requirements of the GMT have been described in the detailed specifications [6]. About 2000 FECs and other equipment are connected to the GMT, a distance of up to 2 km between the nodes has to be covered. In most of the cases a precision of 1 μs is sufficient. However, some equipment like kicker magnets for transferring bunches between machines require nanosecond precision.

Besides supporting control system features like equipment triggering and synchronization, parallel execution, varying machine cycle times and scalability, other key features are the following: *Robustness* - At most one timing event per year may be lost. *Determinism* - Time critical information from must be distributed to the nodes with an upper bound latency. *Redundancy* - Core components of the GMT must be implemented with redundant equipment. *Availability* - The GMT must be capable of distributing events for testing and commissioning equipment, even when the accelerator does not produce beam. *Plan B Execution* - The GMT must react on external signals like interlock signals or malfunctioning equipment by executing predefined alternatives in the schedule. Other important features include integration of the existing machines and control system as well as interfaces to many other subsystems like the interlock system and BuTiS.

DESIGN

The main idea is to build the GMT based on the notion of absolute time. Nodes in a network share the same clock and time. By this, distribution of information and timely triggering are decoupled. This is achieved by preprogramming timing receivers for autonomous execution of actions at a given time and date.

White Rabbit as Field Bus

The new timing system for FAIR is based on a White Rabbit network. The focus of WR is on clock and timestamp distribution, thus synchronizing nodes of a network [1, 7]. WR employs Gigabit-Ethernet, IEEE1588-2008 (PTP), precise knowledge of the link delay and Synchronous Ethernet. The idea is to adjust the clock phase

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(125 MHz carrier frequency) and offset (timestamps in Coordinated Universal Time - UTC or International Atomic Time - TAI) of all network nodes to that of a common grandmaster clock. Today, synchronization in the one nanosecond range with a jitter in the low picoseconds range is achieved using commercial products that have been developed within the Open Hardware Project [8].

Timing System

The main components of the GMT are a *timing master*, a *timing network*, and *timing receiver nodes*.

The timing master acts as a grandmaster clock providing the time for all the nodes in the GMT. It furthermore fulfills the task of the real-time control of the accelerator complex by generating and distributing *timing messages* according the schedule provided by a settings management system. Timing messages are broadcasted to all nodes in the network. The timing master has interfaces to other system of the accelerator control system like the settings management system [9], the interlock system [3] or the the post mortem system [2]. GMT benefits from BuTiS by using it as reference clock input to the grandmaster clock of the timing master. As BuTiS uses a GPS Disciplined Oscillator (GPSDO) for long term stability, the GMT itself uses and distributes timestamps based on GPS time.

A dedicated timing network distinct from the general controls network is required. First, WR-PTP uses the physical carrier signal of GigE for propagation of clock and phase from the timing master to the nodes, requiring dedicated switches. Second, the timing network must have real-time capabilities transmitting timing messages with a guaranteed upper bound latency. Third, the timing network support robustness against loss of packets and bit errors.

FECs are connected to two distinct networks. First, the general purpose network of the accelerator control system is used to transmit set values in order to preconfigure a FEC in advance. Second, the timing receiver, which is typically an interface card connected via the host-bus bridge of a FEC, has a link to the timing network. The main form factor for FECs at FAIR is the Scalable Control Unit (SCU) [10]. As timing receivers receive all timing messages broadcasted by the timing master, they must filter the identifiers, that are contained in the messages stream. Filtering and processing is done in real time. Once a relevant message has been identified, an action is scheduled for execution at a given time and date. An action could be issuing an interrupt request via the host system bus, which triggers a pre-configured real-time action in the front-end software of the FEC. Of course, timing receivers can generate digital signals for direct hardware triggering in cases, where a precision in the order of nanoseconds is required.

IMPLEMENTATION PLAN

From the point of view of the hardware, White Rabbit is quite simple and based on fairly cheap electronic components which are commonly available. WR interface cards can be obtained from different companies. The development of switches for WR networks is completed and such switches will be available as commercial products in 2013. Thus, the challenge for building the FAIR timing system is not so much the development of new technologies but to combine existing technologies using White Rabbit technology as a field-bus. Especially the scaling of the timing system to more than 2000 nodes as required for the FAIR facility must be addressed with care [6].

The solution is to develop the GMT in an iterative and incremental way. Each iteration cycle results in a running system. The first iteration cycle must demonstrate the principal feasibility of critical components, while successive iterations implement additional features until the desired total functionality is reached.

From Existing Machines to Fair

Proton Linac Source In summer 2013 GSI will deliver a complete control system for testing the source of the proton linac, that will later serve as an additional injector into the existing synchrotron SIS18 at GSI/FAIR. At this stage, the timing system will only be a simple pulse generator for a handful of FECs. However, this will be the first productive timing system that uses prototypes of the FAIR timing system, such as a timing master, a timing network and timing receivers.

CRYRING The next step will be a timing system for the CRYRING, a small synchrotron and storage ring located at the Manne Siegbahn Laboratory in Stockholm [11]. This ring will be moved to GSI, where it will be setup next to the Experimental Storage Ring (ESR). One of the motivations behind the CRYRING project is its explicit usage for FAIR development tests. Although the operation of the ring will commence in stand-alone mode, it covers nearly all relevant aspects of an accelerator facility. Thus, it presents an ideal test ground for new sub-systems of the accelerator control system such as the timing system. Here, new development and features for FAIR can be tested without the overhead required for routine operation. It is estimated that between 20 and 50 FECs have to be connected to a first timing system. Although limited in features, deployed components for the CRYRING timing system will be close to the final ones for FAIR.

New Timing System for SIS18 and ESR The timing systems for the proton linac source or CRYRING have been either very small in scale our operated under experimental conditions. Replacing the existing timing system at the synchrotron SIS18 and the storage ring ESR is a important milestone, since the ongoing experimental program requires the timing system to work reliably in routine operation 24/7. The old timing system, which is based on an extension of the MIL-STD-1553 bus, needs to be replaced by the new GMT: A common solution for the timing system for all ring machines should be used to guarantee and efficient transfer of ion bunches from one ring machine to the next.

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Integration of UNILAC Next to the new proton linac, the existing heavy ion linear accelerator UNILAC is the second injector into the FAIR accelerator complex. Here, the existing MIL-based timing system will most likely not be replaced for the reasons of cost and effort. Moreover, the UNILAC is special with respect to timing. First, it is operated at 50 Hz and phase locked to the mains voltage delivered to GSI. Second, the ion sources feeding the UNILAC require fixed repetition rates for reasons such as thermal stability. However, injecting the UNILAC beam into the SIS18 requires linking the UNILAC timing to the schedule of the FAIR accelerator complex. This must be achieved and tested prior to commissioning the FAIR facility.

Final Timing System All of the previous instances of the new GMT had different aspects: Proof of principle at the proton linac source, prototyping and development of final solutions at the CRYRING and reliability of routine operation at the SIS18 and the ESR. One important step towards the final timing system is the combination of all these aspects. This is eased, since the timing master and the first two layers of switches will be physically located in an existing building close to the SIS18. This allows to set up first components of the timing master for CRYRING, SIS18 and ESR already. By this, the timing master, its infrastructure and its interfaces will be continuously developed, improved and tested at its final location over a few years.

Another important step is to address the issue of scaling the new GMT to the size required for the final FAIR facility. As it is planned to purchase the equipment not just before FAIR machine commissioning but over a period of several years, scalability can be addressed and tested in several steps. One option would be to use test areas in buildings of the existing facility.

STATUS

During the past years, the main focus of the work done at GSI has been on the design, specification and prototyping of components for the GMT.

As the timing master for the FAIR facility will be located in an existing building at GSI, space was allocated and racks for electronics have been set up. First cables for fiber links have been laid to connect the timing master to three different locations on the GSI campus. GPS antennas and a GPSDO have been installed and are being commissioned. The GPSDO serves as a stabilized external reference clock with low phase noise and provides GPS timestamps. At the same location, a White Rabbit switch has been installed which synchronizes to the GPSDO. Today, this switch can today be used as grand-master clock for first tests to supply three other locations at GSI with White Rabbit links. Connected to these links are White Rabbit receiver nodes.

White Rabbit PTP just provides clock and time synchronisation. However, timing receivers for the GMT need to implement the functionality to schedule and execute actions for synchronizing the accelerator equipment. This is a major effort, which has already been addressed. As one of the results, the so-called *GSI Timing Starter Kit* has been developed which already today allows features like digital outputs at a pre-programmed time and date as well as latching of timestamps [12]. The SCU serves as the main platform for the development of timing receivers at GSI.

SUMMARY AND OUTLOOK

A new general machine timing system for FAIR is presently being developed in iteration cycles, where each iteration provides a functional timing system focusing on a certain aspect of the final timing system. The first iteration yielded a timing starter kit. The next iterations will implement timing system for the source of the FAIR proton linac, followed by the CRYRING at GSI. The replacement of the existing timing system at the SIS18 and the ESR combined with addressing scalability will pave the way to the new timing system for the FAIR facility.

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