A DISTRIBUTED CAN BUS BASED EMBEDDED CONTROL SYSTEM FOR 750 keV DC ACCELERATOR

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Abstract

This paper describes a distributed embedded system that uses a high performance mixed signal controller C8051F040 for its DAQ nodes and is based on CAN bus protocol for remote monitoring and controlling of various subsystems of 750 keV DC accelerator based irradiation facility at RRCAT, Indore. A PC with integrated PCI CAN card communicates with intelligent DAQ nodes over CAN bus and each node is interfaced with a subsystem. An opto isolated SN65HVD230 CAN driver is interfaced between each node and physical bus. Remote frames and message prioritising are used for efficient control. The PC application is developed using LabVIEW 8.6. The proposed system is more reliable and noise immune as compared to previously used systems that initially used a centralized system based on C8051 controller. This was then upgraded to a distributed system that used microcontroller AduC812 and communicated over RS485 link. The new system has been integrated and tested satisfactorily for its designed performance with test jigs that simulated the actual subsystems with a bus length of 75 meters. First the complete scheme of the system is presented, and then the hardware and software designs are discussed.

INTRODUCTION

A 750 keV 5 mA electron beam accelerator has been developed and commissioned for industrial processing application at RRCAT, Indore. In this accelerator a directly heated diode gun is used as an electron emitter, which is floating at minus 750 keV DC with respect to the earth. The accelerating voltage for the accelerator is generated using a 12-stage symmetrical voltage multiplier stack. The input to the multiplier stack is derived from a high frequency resonant inverter through ferrite core high voltage transformer. The inverter output and hence the high voltage is varied by controlling the DC bus voltage of a three phase fully controlled converter which feeds the inverter. The filament power supply is derived from the top of the multiplier stack across its isolation columns, which has an inherent isolation of 750 kV with respect to the earth. The accelerated electron beam is focused by two focusing coils and is made to scan the material under process with the help of a scanning magnet field. The high voltage stack, the accelerating column and the filament power supply are closed in a pressure vessel, which is filled with SF6 gas at a pressure of 5 atmospheres. The accelerator, which is under operation at RRCAT, Indore since 2002 is being used for research and development in the field of irradiation processing.

The PC based control and monitoring system of this DC Accelerator is being upgraded for easier operation and better control and monitoring of different parameters of the accelerator and allied subsystems.

HARDWARE DESCRIPTION

The PC based system, controls and monitors different parameters of various subsystems of the DC accelerator which includes different power supplies, various control units, transducers, on/off controls, search and scram system etc. The analog parameters, which are being controlled and monitored, include accelerating voltage, emission current, filament current, scanning coil current among others.

In the proposed scheme that uses a distributed control system communicating over CAN(Controller Area Network) bus, each power supply and subsystem which is to be monitored and controlled through PC is interfaced with a data acquisition card (DAQ node). The DAQ node implements a microconverter C8051F040 from Silicon laboratories, which has an inbuilt high speed 8051-compatible CIP-51 core and a CAN controller. It also has a 12 bit ADC with 8-channel analog multiplexer and two 12-bit DACs. All analog inputs are taken in through differential amplifiers to reduce the effects of common mode noise. The DAQ node can also monitor eight digital inputs and control eight digital outputs.

All the DAQ nodes are connected on a common CAN bus line. The control PC is connected on the same CAN bus through an integrated PCI CAN card. CAN bus message based communication protocol is used for communication between PC and the DAQ nodes.

Each DAQ node will be allocated messages with specific addresses and will act as a slave. The PC is the master and communicates with the power supplies and other subsystems through this known message addresses using normal and remote frames. The data will be embedded into the well-framed message packets. As a result of the content-oriented addressing scheme, a high degree of system and configuration flexibility is achieved.

CAN is a distributed serial bus system widely used in industrial control applications, where robust environment exists. It provides high level of data integrity and automatic bus arbitration. It supports a multi-master hierarchy, which allows building intelligent and redundant systems with broadcast communication. It provides sophisticated error detecting mechanisms and re-transmission of faulty messages. For error detection the CAN protocol implements three mechanisms at the message level: Cyclic Redundancy Check (CRC), Frame check, ACK errors. The CAN protocol also implements two mechanisms for error detection at the bit level: Monitoring: Each station that transmits also observes the bus level and thus detects difference between the bit sent

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and the bit received. Bit stuffing: The bit representation used by CAN is "Non Return to Zero (NRZ)" coding. The synchronization edges are generated by means of bit stuffing. This stuff bit has a complementary value, which is removed by the receivers.

It is easy to add stations to an existing CAN network without making any hardware or software modifications to the present stations as long as the new stations are purely receivers. This allows for a modular concept and also permits the reception of multiple data and the synchronization of distributed processes. Data transmission is not based on the availability of specific types of stations allowing simple servicing and upgrading of the network.

CAN bus supports lowest two layers of OSI reference model namely physical layer and data link layer. Physical layer is implemented by using opto isolated SN65HVD230 CAN transceiver from Texas Instruments and data link layer is implemented by inbuilt CAN controller as shown in Figure 1.

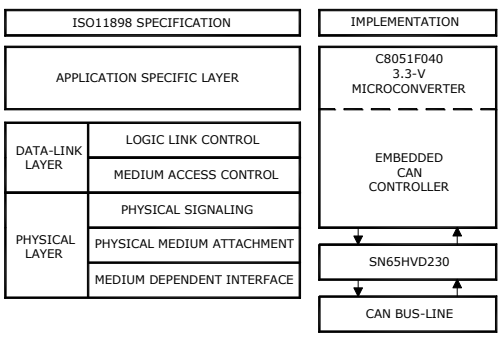

Figure 1 : The Layered ISO 11898 Standard Architecture.

The CAN transceiver employs the CAN serial communication physical layer in accordance with the ISO 11898 standard and provides differential transmit capability to the bus and differential receive capability to a CAN controller at speeds up to 1 Mbps as illustrated in Figure 2.

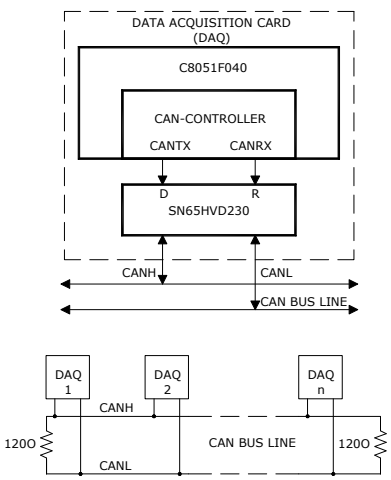

Figure 2: Details of typical CAN DAQ node.

ISO 11898 is the international standard for high-speed serial communication using the CAN bus protocol. It supports multimaster operation, real-time control, programmable data rates and powerful redundant error checking procedures that provide reliable data transmission. It is suited for networking intelligent devices as well as sensors and actuators within the rugged electrical environment of a machine chassis or factory floor.

A DB-9 connector is provided on the card to facilitate serial connections to the CAN interface on the C8051F040. The DAQ card has additional communication interface for opto isolated RS485 based communication. The communication protocol can be selected as either CAN bus or RS485 by switching the jumper settings. The opto isolation reduces the problem of noise interference and ground lifting due to ground loops. The DAQ card also has a JTAG connector that provides access to the JTAG pins of the C8051F040. It is used to connect the USB Debug Adapter to the DAQ board for in-circuit non-intrusive debugging and Flash programming.

The control software is written into 64k bytes of in-system programmable FLASH memory. Figure 3 shows the schematic of the proposed control system.

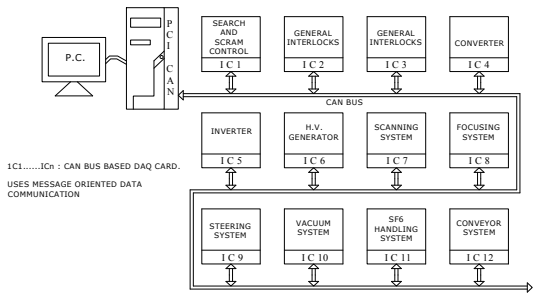

Figure 3: Schematic of the control system.

SOFTWARE DESCRIPTION

Two distinct application softwares are being developed, the microcontroller firmware application and the host PC application. The microcontroller firmware is written in 'C' using KEIL 'C' cross compiler. The program is structured into various modules for carrying out different tasks like CAN intialization, setting up of ADC/DAC, handling digital I/O, interrupts, transmission, reception and decoding of CAN frames.

The PC application and its GUI interface is being developed using LabVIEW 8.6 from National Instruments, for multiple reasons like easy development, debugging and maintenance, excellent windows based graphical user interface and strong support for CAN bus based serial communication.

The PC is used to control the on-off operations or set references of different power supplies and other subsystems and display different parametric values and the status of the machine. The PC starts the system in the search mode and doesn't enter into operation mode till all the pre specified safety and operational conditions are met.

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EARLIER CONTROL SCHEMES

Initial scheme [1] employed a single centralized micro-controller crate and used a number of Input, Output, ADC and DAC cards for communication with various subsystems. The micro-controller system then communicated with PC through RS232 serial link. The software including its GUI for the PC operation was developed using C++ programming language, which imposed several programming limitations.

It was then upgraded to a distributed control system [2] based on RS485 where each subsystem to be controlled through PC was equipped with a AduC812 based micro-controller card and was interfaced to PC through a common RS485 line. Each interface card had a unique predefined address. A RS485 to RS232 and RS232 to RS485 converter was used at PC end. The Control Software for PC was written in LabVIEW 7.1. PC was master and controllers operated as slaves

This system suffered from several shortcomings. Data frame creation and decoding was implemented at software level instead of hardware level both in microcontroller and LabVIEW code due to missing data link layer. To achieve reliable data transmission additional coding was required to implement data checking and retransmission capability. Analog inputs on interface card required additional filtering to minimize common mode noises. The need for better debugging capabilities for microconverter coding was felt.

With low data handling requirements and above mentioned required features, a CAN bus based system suited the application. Hence microconverter "C8051F040" was chosen as it has 8051 core with inbuilt CAN controller, 12 bit ADCs & DACs, sufficient IO ports and JTAG interface.

TESTS AND RESULTS

CAN bus based data acquisition cards have been designed and developed. The embedded system was tested thoroughly and performance at component and module level was observed. Each module was tested individually for its performance with simulated inputs. A test bench was developed to test the system. Initial test codes for controller card and software application for PC operations have been developed. The system is being tested and it is possible to both monitor and control the analog and digital controls of the test bench through the LabVIEW based GUI on the PC. Data is being transferred between the PC and the CAN card using CAN bus protocol at 1 Mbps. Data transfer over a cable length of 75 meters has been tested successfully at 500 kbps. The new design has given us the capability of adding more subsystems (like any additional power supply etc.) as and when required. It requires addition of a new DAQ card with allocation of new message addresses and hooking it on the existing CAN bus line.

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