FPGA BASED AMPLITUDE CONTROL SYSTEM FOR ACCELERATING CAVITIES

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Abstract

The FPGA (Field Programmable Gate Array) based digital controller has been implemented for low level RF voltage control of a 650 MHz cavity. Implementing amplitude control in a compact single board solution, FPGA is chosen. The Superconducting cavity is designed to be operated at 650 MHz and 30kW, CW mode. The voltage from pick-up coil has been fed to the controller after down conversion; the signal is digitized using high speed ADCs. The controller has been simulated with different set points and gain parameters. The FPGA signal processing has been simulated according to the required strategy of the reference controller. Some simulation results have been presented for different cavity operational conditions.

BRIEF THEORY OF TRANSFER FUNCTION

Suppose the input to the cavity be an amplitude modulated (AM) signal with carrier frequency ω_c, exactly tuned to the cavity. The AM input signal is expressed mathematically as:

$$V_i = A_i[1 + a_i(t)]\cos\omega_c t$$

The output of cavity will also be an AM signal with carrier same as above and is expressed mathematically as:

$$V_o = A_o[1 + a_o(t)]\cos\omega_c t$$

On demodulating the output AM signal we will get the output baseband signal $a_o(t)$. It can be verified that the cavity action on baseband input signal $a_i(t)$ is a low pass filter whose cut-off depends upon the cavity resonant frequency and quality factor. Thus the baseband transfer function of the cavity model can be expressed as:

$$G(s) = \frac{a_o(s)}{a_i(s)} = \frac{1}{1 + s/\sigma} \quad \text{, where } \sigma = \frac{\omega_r}{2Q_L}$$

SYSTEM LEVEL IMPLEMENTATION ON FPGA

The implementation of the cavity control loop requires a modulator and demodulator along with a controller with an external set point and gain. Figure 1 shows the system level block diagram. There are three parts in the block diagram comprising of firmware, RF cavity and the portion that implemented outside the FPGA. The components outside the FPGA firmware are the ADC-DAC add-on modules, PC running the software and the RF cavity system.

The control loop parameters like set-point, gain and loop control action are controlled by the user through an RS232 serial port. Control loop implemented using FPGA firmware and a proportional controller at the current stage as in Figure 2, the set-point is compared with the demodulated cavity output in FPGA, and the error data after multiplying by the gain parameter 'G', goes outside the FPGA for modulation since the DAC input is AC-coupled. The DAC output after modulation with a 5 MHz carrier goes into the cavity.

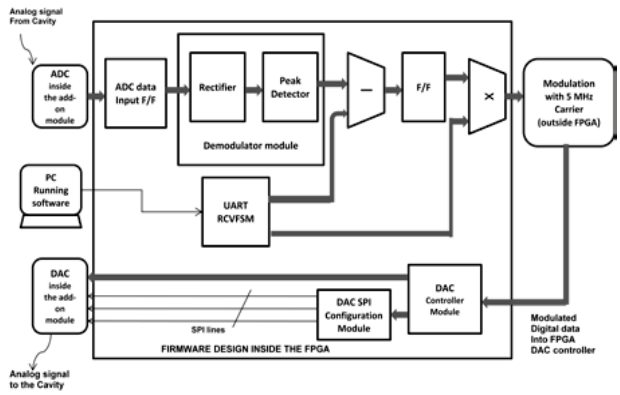

Figure 1: System level block diagram.

FPGA Hardware and Firmware Details

Hardware details: The hardware components of the implementation mainly consist of a FPGA (Virtex4) MB development board and an ADC-DAC add-on module. ADC accepts analog input of 1.8 Vpp, and outputs digital data in 2's complement format. It has a conversion delay of $17.5 \times T_{CLK}$.ADC output clock acts as the FPGA clock @ 100 MHz; DAC accepts a 16-bit digital input in 2's complement format and outputs pk-pk value of 500mV.

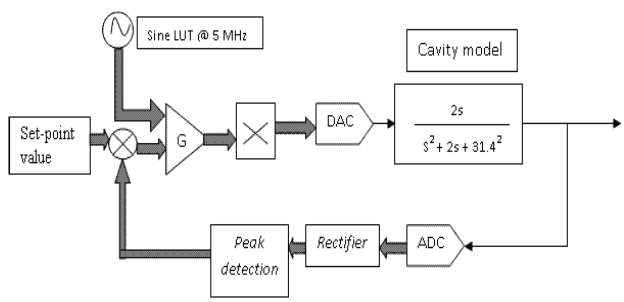

Figure 2: Block diagram of the control loop implementation using FPGA.

Firmware details: The FPGA firmware is designed to capture the high speed ADC data followed by its demodulation and then applying the digital control action.

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Demodulating an AM signal requires a rectifier followed by the envelope detector with a peak detector module. The peak detector module acts as an envelope detector. The rectifier is introduced just to clip out the negative value data so as to reduce the number of data samples in a window. The peak detector is based on window based peak detection. Controller, it compares the demodulated output with the set-point value and the gain. Modulation of the controller output is done outside the FPGA, and the modulated signal is given back into FPGA for conversion to analog value using DAC inside the add-on module.

SIMULATION RESULTS

The above control loop has been simulated in MATLAB Simulink simulation tool. Various parameters are downscaled by factor of 10^6 for convenience. The carrier level control loop in Figure 2 can be converted to its equivalent baseband model by replacing the components.

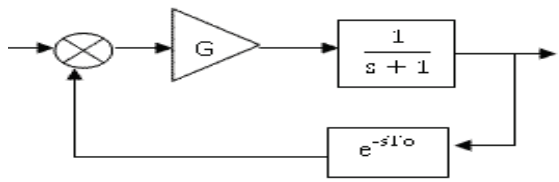

Figure 3: Baseband equivalent model of control loop.

It can be shown in Figure 3; the output stability is limited by the gain G and delay T_0. The simulation output of actual carrier level and baseband model is shown in Figure 4(a) to 4(e) for various values of gain and delays. The gain and set-point of carrier level model is limited by product G x S.P. <32767 (for 16-bit DAC). All the simulation outputs in the following figures are having a set- point of decimal 3000 for the carrier level model and a set-point of unity for the baseband model.

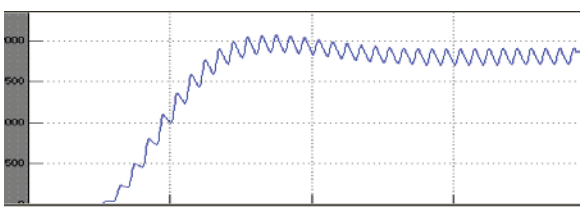

Figure 4(a): Carrier model Simulink output, G=5.

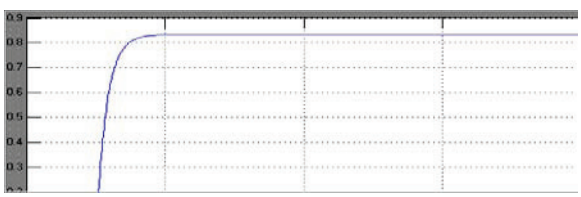

Figure 4(b): Baseband model Simulink output, G=5, T_0=0.02 seconds.

As seen from the Figure4 (a), the output is at the demodulator in response to the step decimal input of 3000. The output gets stabilized to 1800 value. The output shows little ripple due to the carrier noise after demodulation. The ripple is of order of 5.5 mV for ADC input range of 1.8Vpp, which amounts to 0.28% only. Figure 4(b) shows the similar response to the step input to the equivalent baseband model. The output is a factor 5/6 of input i.e. 0.833.

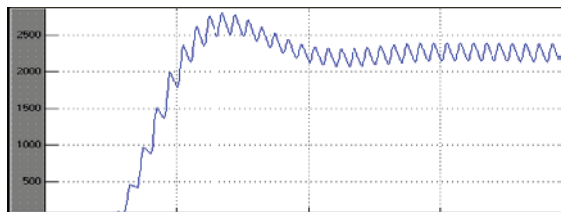

Figure 4(c): Carrier model Simulink output, G= 10.

Similarly, the output response of Figure 4 (c) shows that if gain is increased by 10, then output gets stabilized to 2300. The output shows transient oscillatory response due to the decrease in stability caused by the increase of gain. Similar oscillatory response we get in the baseband model with gain of 10, and delay 0.05 seconds.

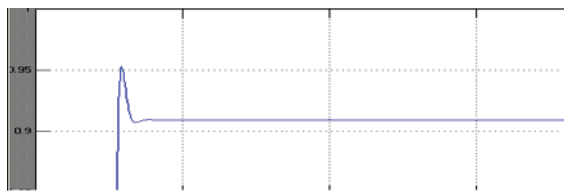

Figure 4(d): Baseband model Simulink output, G=10, T_o=0.05 seconds.

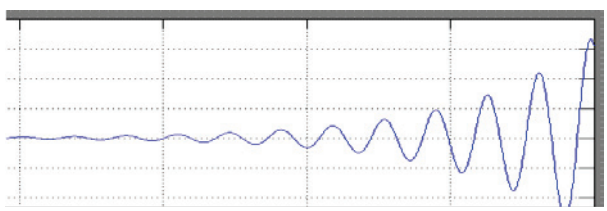

Figure 4(e): Baseband model Simulink output, G=10, T_o=0.2 seconds.

Figure 4(e) shows the output of baseband model with an increased delay gets unstable, while gain remains unchanged.

TESTING DEMODULATOR

The control loop shown in figure 2 has been simulated. The demodulator along with the controller is tested in the lab, and found working. As shown in the Figure 5, the AM signal is applied to the ADC input, and after demodulation in FPGA firmware, and the controller section, the data is fed directly to DAC to test firmware implementation. The modulation is bypassed in this testing since it has to be implemented outside the FPGA.

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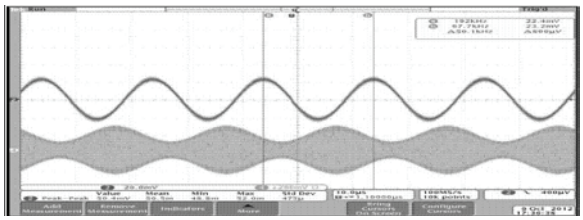

Figure 5: A 5 MHz carrier signal modulated by a 50 kHz baseband sine wave demodulated by a demodulator module implemented in FPGA.

The simulation work was complete and the model is codified in vhdl. The design is not yet put on the actual cavity. The actual set-up and the performance study are undergoing. The concept and the details of the work have been taken into account from [1, 2, 3, 4].

REFERENCES

[1] Tomasz Czarski, Krzysztof Pozniak, Ryszard Romaniuk, Instt. of Electronic Systems, Warsaw University of Technology, Poland, Stefan Simrock, DESY, TESLA, Hamburg, Germany, "Cavity control system model simulations for TESLA linear accelerator".

[2] A. Gallo, INFN LNF, "Basics of RF electronics", CERN Yellow Report CERN-2011-007, pp. 223-275.

[3] Erk Jensen, "RF Cavity Design", CERN BE/RF, CERN Accelerator School, Accelerator Physics, Chios 2011.

[4] Wojcieh M. Zabolotny, et al, "FPGA based Cavity Simulation for Tesla Test Facility", Tesla Report 2003-22.

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ISBN 978-3-95450-124-3